DESIGN OF COMPONENTS FOR MMWAVE PHASED ARRAY IN DEEP SUBMICRON CMOS TECHNOLOGY

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DESIGN OF COMPONENTS FOR MMWAVE PHASED ARRAY IN DEEP SUBMICRON CMOS TECHNOLOGY

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To my parents and sisters

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TABLE OF CONTENTS

LIST OF TABLES

LIST OF FIGURES

SUMMARY

With the advancement in wireless communication, there has been a lot of overlap in the frequency spectrum used by different applications in the lower frequency band. Also there is an ever-increasing demand for high-speed wireless data transfer. Due to the aforementioned reasons, a lot of work is being done recently in the unlicensed 60GHz bandwidth due to the high data rates it can support. But it is tough to achieve long-range point-to-point transmission at this frequency due to the limited output power and high path losses. A phased array system is a viable solution at these mmWave frequencies to achieve highly directive long-range point-to-point communication. The objective of this research is the design and implementation of phase shifters, VCO and LNA for mmWave phased array system.

In this work, active and passive quadrature generation schemes integrated with a vector modulator have been proposed that can be used to produce arbitrary phase shift with a deterministic resolution at the LO signal. Also, alternate IF and PLL based phase shifting schemes for a mmWave phased array system have been proposed. A complete design procedure from parasitic modeling of devices to verification of the design using EM simulations has been discussed in this work. The simulation results are compared with actual measurement results from the fabricated chip and the performance of the various circuits has been analyzed. Furthermore, the designs of VCO and low noise amplifier to be used in the mmWave phased array system are discussed here.

CHAPTER I

INTRODUCTION

1.1 Motivation

In the past few decades, there has been a tremendous growth in wireless technologies. The rapid advancement in semiconductor technologies together with the high level of integration that is feasible in Si processes has been the main driving force behind this growth in the wireless technologies. With the exponential increase in the amount of data that needs to be transferred between users, there has been a lot of thrust in the development of new architectures and transmission at much higher frequencies.

Though use of higher modulation schemes like 256-QAM can increase the data transmission rate, the required signal level, system linearity and noise performance specifications become very stringent in these systems. Hence, the focus has now shifted towards wireless transmission at much higher frequencies, which can support a much higher modulation bandwidth. In this aspect, the use of unlicensed 60GHz frequency spectrum for short-range high data rate transmission is an attractive option.

In the past, these millimeter wave(mmWave) systems have been designed using III-V compound semiconductor technologies. Though they have excellent performance at mmWave frequency, they are expensive, exhibit lower yield and cannot be integrated directly with the digital baseband circuitry. With the advancement in standard CMOS process technologies, these mmWave systems can now be implemented in standard CMOS process at a much lower cost with higher integration capability.

Though the implementation of mmWave circuits in standard CMOS processes has a number of advantages, they have not yet completely replaced the compound semiconductor process technologies due to their inferior power output capability and poor noise performance. Phased array, a class of multiple antenna systems, is one viable solution, which can be used to overcome the aforementioned drawbacks. In a phased array system, the

electronic beam steering is achieved by varying the relative phase of the transmitted signals between the adjacent transmitter elements. The steered beam adds coherently in one particular direction increasing the effective power transmitted in that direction. If the power output from each transmitter is P watts, the EIRP in the main beam direction of a phased array system(n elements) is n^2P watts [10]. Apart from increase in EIRP, they can also be used to improve directivity of transmitted waves, SNR of the received signals and sensitivity of the receiver system. Some of the applications of a phased array system are shown below in Figure 1.

Figure 1: Applications of phased array system

Some of the essential components in a phased array system are phase shifter, LO generation circuitry, low noise amplifier, power amplifier and mixer. The focus of this research work is on the design of phase shifters, VCO's, QVCO's and low noise amplifiers for a phased array system.

1.2 Organization

Chapter 2 gives a brief overview of the different phased array system implementations. Chapter 3 explains the different modeling issues that need to be considered for design at mmWave frequency. Chapter 4, 5 and 6 discusses the different types of LO phase shifters that have been designed. Chapter 7 and 8 discusses the design of LO generation circuitry and low noise amplifier for a phased array system.

CHAPTER II

PHASED ARRAY ARCHITECTURE

A phased array system consists of a group of antennas, which are fed with signals whose relative phases are varied in such a way that the radiated signals combine constructively in the desired direction and are suppressed in the other directions. In section 2.1, an introduction to phased array system is provided. In section 2.2, the operating principle and in section 2.3, the different phased array system architectures available are explained in detail.

2.1 Introduction

Since the early 90's, there has been a lot of thrust in the design of highly directive antennas for long-range communication and radar applications. Though the increase in antenna size improves the directivity [2], this method is not suitable for generation of very fine beams due to the large antenna size required. Also, in radar applications, the beam needs to be steered rapidly, which is difficult with a large antenna. These limitations are overcome by using a phased array system that can generate and rapidly steer highly directive beam. These systems can be used with omni directional antennas reducing the size and complexity of antenna design. A phased array system achieves the required beam steering and directivity by varying the relative phases of the signals transmitted by the different antenna elements. The first electronic implementation of such a phased array system was done during the World War II. Apart from defense applications [16], the phased array systems can also be used in long-range communication [18], radio astronomy [3], vehicle collision avoidance systems [27], medical imaging [25] and non-line of sight communication.

In a phased array transmitter, the output signals from the different unit elements are phase shifted to reinforce in one particular direction while they get cancelled in the other directions. Since the signals add up constructively in the direction of interest, it increases the effective output power/EIRP in that direction. This can be used to increase the range

of the wireless link in the direction of interest. Also, since the signals add up destructively in other directions, there is very little interference from/to other transceivers operating in the same frequency but in other directions.

In a phased array receiver, the received signals from the different unit elements are phase shifted for phase alignment and then combined. Since the signal component in all the unit elements are correlated, they add up in the voltage domain. But, the noise component in each unit element is uncorrelated and they add up in power domain. Therefore, the SNR improves by a factor of N as shown below.

$$SNR_{in,i} = \frac{V_0^2}{n_i} \qquad for\ i = 0\ to\ N-1 \tag{1}$$

After Combining

$$SNR_{out} = \frac{N^2 V_0^2}{N n_0} = N\frac{V_0^2}{n_0} = N.SNR_{in,0} \tag{2}$$

2.2 Principle of Operation

The principle of operation of a phased array system can be explained using a linear array [20] shown below in Figure 2.

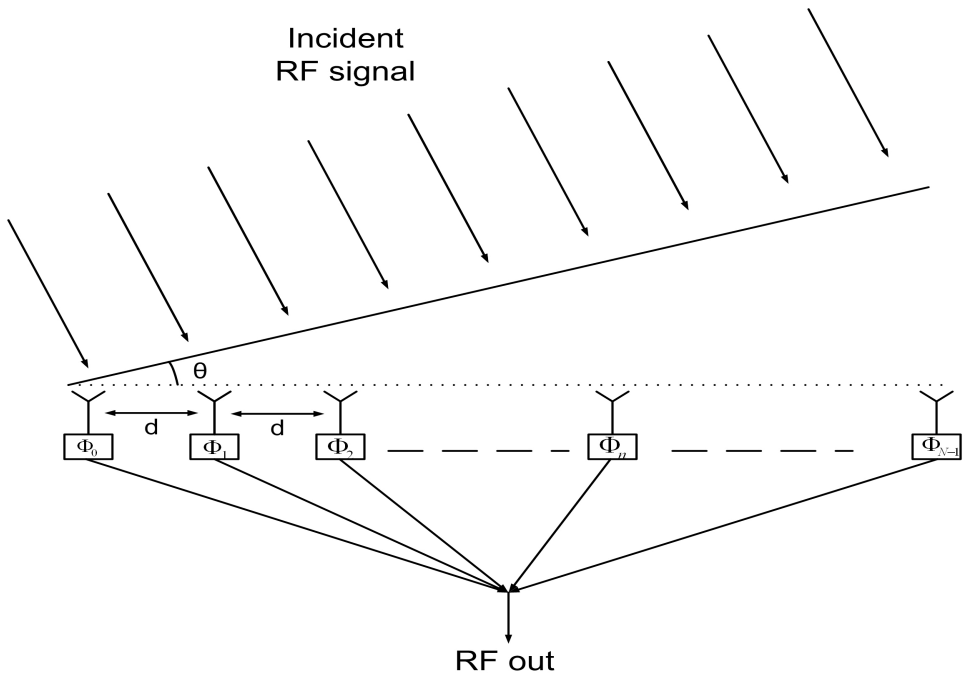


Figure 2: Linear receiver array

Consider a beam incident at an angle 'θ' on a linear array with 'N' elements each separated by a distance, d. The delay difference between the signal incident at element '0' and element 'n' is given by equation(3).

$$n\tau = \frac{nd\sin\theta}{c} \tag{3}$$

Let $\Phi(n)$ be the phase shift at unit element 'n' before combining. Then, the output signal at the n^{th} element is given as

$$V_n(t) = V_o(t - n\tau).\cos(W_{rf}(t - n\tau) - \Phi(n)) \tag{4}$$

Using the above relationship, the combiner output signal can be given as

$$V_{out}(t) = \sum_{n=0}^{N-1} V_o(t - n\tau).\cos(W_{rf}(t - n\tau) - \Phi(n)) \tag{5}$$

Since the modulation bandwidth is far less than W_{rf} the above equation (5) can be rewritten as

$$V_{out}(t) = V_o(t).\sum_{n=0}^{N-1} \cos(W_{rf}(t - n\tau) - \Phi(n)) \tag{6}$$

If the phase shifts in the individual units are arranged in such a way that Φ(n)=(N-n)Φ, we can rewrite equation (6) as

$$V_{out}(t) = Re\left(V_o(t).\sum_{n=0}^{N-1} e^{j\left(W_{rf}t - W_{rf}n\tau - N\Phi + n\Phi\right)}\right) \tag{7}$$

$$V_{out}(t) = Re\left(V_o(t).e^{j\left(W_{rf}t - N\Phi\right)}.\sum_{n=0}^{N-1} e^{jn(\Phi - W_{rf}\tau)}\right) \tag{8}$$

The absolute value of the above equation is given as

$$|V_{out}(t)| = \left|\frac{\sin\frac{N\left(W_{rf}\tau - \Phi\right)}{2}}{\sin\frac{W_{rf}\tau - \Phi}{2}}.V_o(t)\right| \tag{9}$$

with a maximum value at

$$\Phi = W_{rf}.\tau = W_{rf}\frac{d\sin\theta}{c} \tag{10}$$

From the implementation and coupling perspective, increasing the spacing, d, between the array elements is favourable. But, for a spacing more than λ the grating lobes deteriorate the array pattern. Hence, the spacing factor is usually kept between $\lambda/2$ to λ for the different scaling angles required. From the above derivation, it is evident that for a steering angle of -90 to +90 degrees, the phase shift in each element needs to vary from 0 to 360 degrees. This is one of the stringent constraints for a phase shifter design.

2.3 Phased Array Architectures

A phased array system achieves beam steering by radiating/receiving the same signal at different phases from the different antennas [11], [5], [24]. The required phase shift can be applied at any point in the transmitter/receiver chain like the RF or the LO or the IF or the baseband [11], [32], [14]. Each of the above mechanisms has their own tradeoffs in terms of the number of signals that need to be routed to unit elements, total power consumption, area occupied by unit element, potential for scalability and robustness of the design.

2.3.1 RF phase shifting

RF phase shifter based phased array system consists of a single up/down conversion stage followed by a number of RF phase shifters and power amplifiers/LNAs. The RF signal is routed symmetrically to each unit element creating a common phase reference plane for the entire system. A simplified block diagram of a phased array system using RF phase shifters for beam forming is shown below in Figure 3.

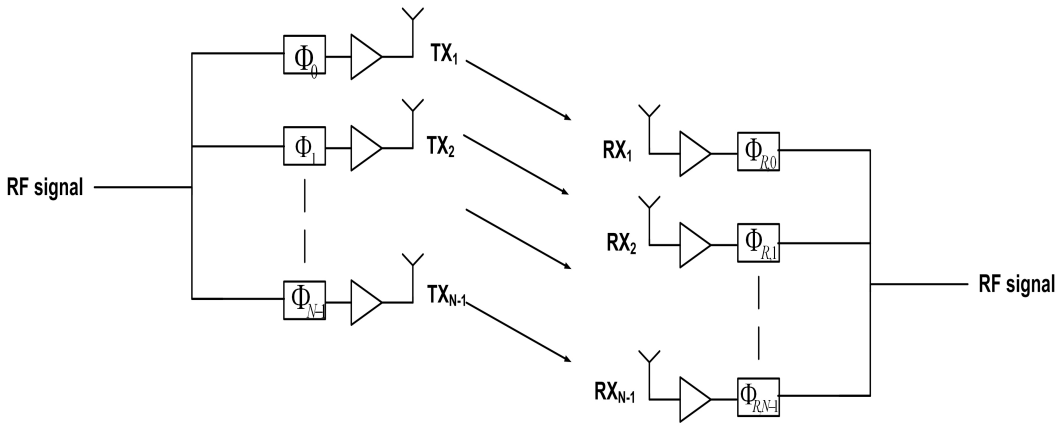


Figure 3: Simplified block diagram of RF phase shifter based phased array architecture

Since the RF phase shifter lies in the signal path, the non-idealities in the RF phase shifter directly affect the system performance by degrading the SNR, distorting the signal constellation and reducing/limiting the maximum output power level. Hence, the specifications on the RF phase shifter performance parameters like the gain, linearity, bandwidth, RMS gain & phase error and group delay are very stringent.

2.3.2 LO phase shifting

In a LO phase shifter based phased array system, each unit element consists of a mmWave up/down convertor, PA/LNA and a LO phase shifter. The LO and the IF/baseband signals are routed symmetrically to each unit element creating a common phase reference plane for the entire system. A simplified block diagram of a phased array system using LO phase shifters for beam forming is shown below in Figure 4.

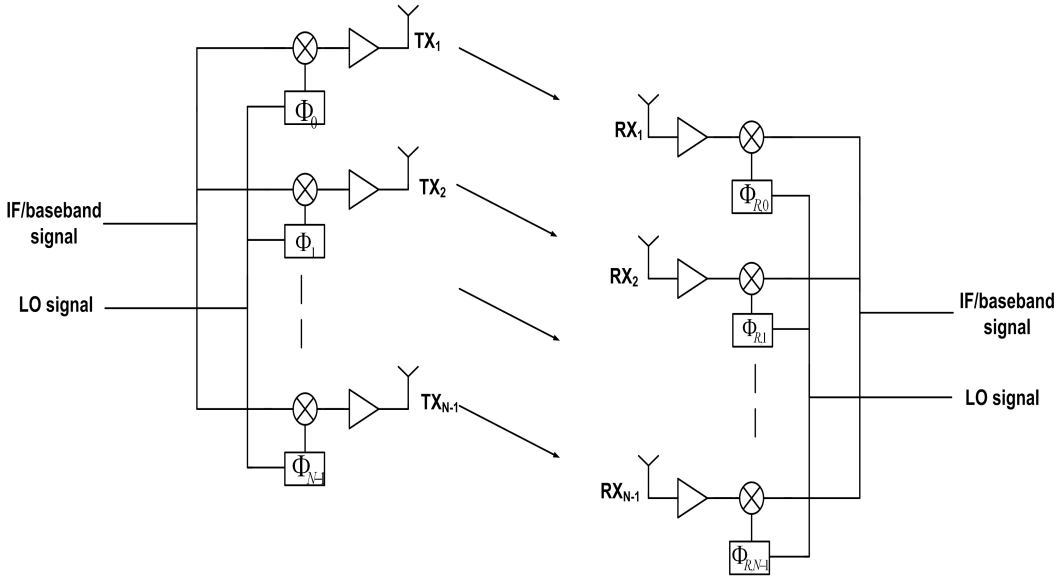


Figure 4: Simplified block diagram of LO phase shifter based phased array architecture

Since the phase shifter lies in the LO chain, the non-idealities in the LO phase shifter does not directly affect the system performance. Hence, the specifications on the LO phase shifter performance parameters are far more relaxed. Some of the common LO phase shifting approaches are shown in Table 1.

Table 1: Types of LO phase shifters

Performance metric	Passive PS [28]	Vector modulator [30]	Injection locked VCO [26]	Coupled oscillators [31]	VM with inj. VCO
Insertion loss	High	Low	Low	Low	Low
Amplitude balance	Bad	Good	Good	Good	Good
Phase shift	0^o to 360^o (tough)	0^o to 360^o	-90^o to 90^o	-90^o to 90^o	0^o to 360^o
Arbitrary phase shift	Yes	Yes	Yes	No	Yes
Power consumption	0	Moderate	High	High	Very High

A variant of the LO phase shifting architecture is the proposed IF phase shifting architecture where the phase shifter is placed in the IF chain [22]. Since most of the modern communication systems support n-QAM modulation, a quadrature IF is used for up/ down conversion which enables use of IQ summer based architectures (Vector Modulator) for phase shifting [23]. IF phase shifters are easier to implement compared to LO phase shifters due to their relatively low frequency operation. But, the unit elements are complex and have higher power consumption.

2.3.3 Baseband phase shifting

In a baseband phase shifter based phased array system, each unit element consists of an entire transmitter/receiver system. The LO signal is routed symmetrically to each unit element, creating a common phase reference plane for the entire system. A simplified block diagram of a phased array system using baseband phase shifter is shown in Figure 5.

Since the baseband phase shifter is placed in the signal chain, the specifications on its performance parameters are very stringent. Apart from beam forming, the RX baseband phase shifter can also be used for feedforward demodulation of QPSK and n-QAM signals from IQ mixer output.

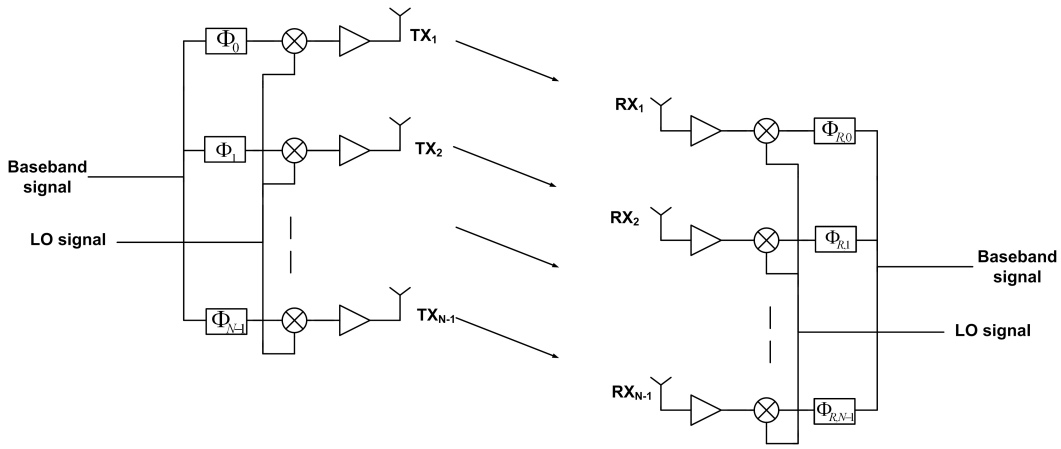


Figure 5: Simplified block diagram of baseband phase shifter based phased array architecture

2.3.4 Novel PLL based phase shifting

Apart from RF, LO and baseband phase shifting, a phased array system can also be implemented using a novel PLL based phase shifter [29]. Here, each unit element consists of an entire transmitter/receiver chain and a PLL. The reference and the baseband signals are routed symmetrically to each unit element, creating a common phase reference plane for the entire system. The schematic of the proposed architecture is shown in Figure 6.

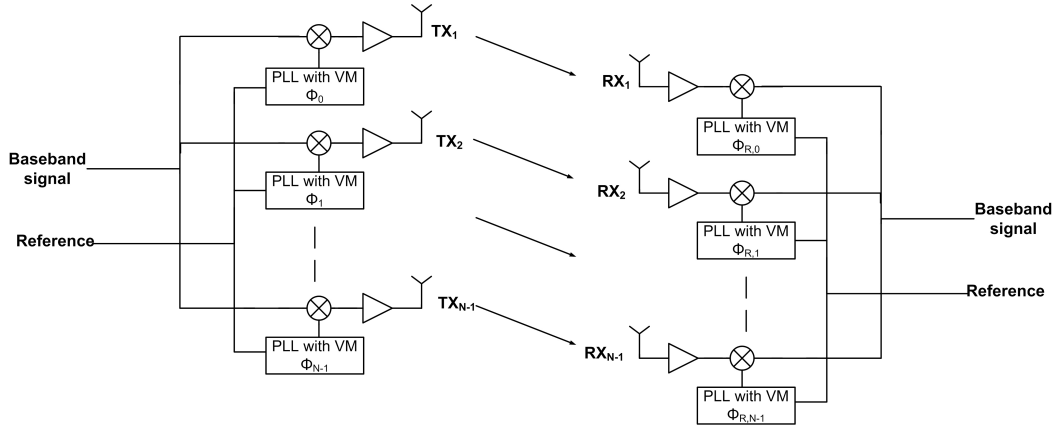


Figure 6: Simplified block diagram of PLL phase shifter based phased array architecture

2.3.4.1 Principle

We know that, any time delay inside the PLL loop is compensated for by a corresponding time delay at the VCO output. This principle can be used to produce the required phase

shift at the PLL output by using a divider/vector-modulator based phase shifter in the PLL loop. The vector modulator uses master slave divider quadrature output to produce the required phase shift. Since the quadrature signals produced by the master slave dividers are well balanced, the phase shift response is linear. A prescaler can be used to lower the operating frequency and enable easier implementation of the divider/vector modulator based phase shifter. If the vector modulator is present at the output of the divided by N divider, the phase shift at the PLL output is N times the phase shift produced by the vector modulator. The block diagram of a PLL embedded with a phase shifter is shown below in Figure 7.

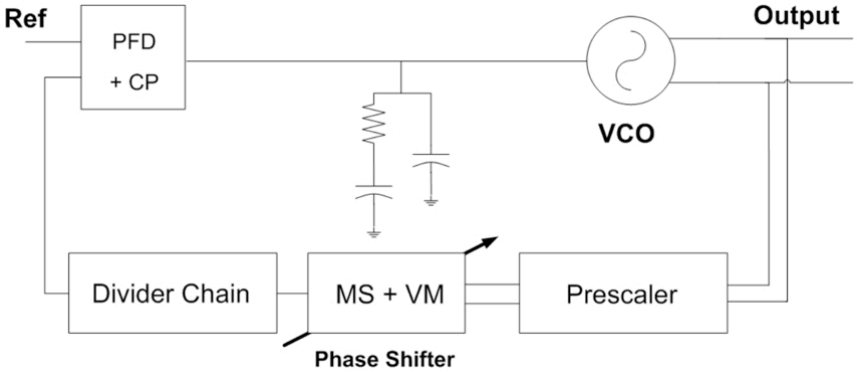


Figure 7: Simplified block diagram of PLL based phase shifter

In this research work, the design of components for a LO phase shifter based phased array system is presented. Here, the components are designed for two different frequency plans for a 60GHz system. The LO phase shifters and the LNA are designed for a 60GHz system with a LO frequency of 53GHz and an IF frequency of 7GHz. The LO generation circuitry namely, a push-push VCO and QVCO are designed for a system with a LO and IF frequency of 48GHz and 13GHz respectively.

CHAPTER III

COMPONENT MODELING

The main challenge in millimeter wave design is the accurate prediction of performance of the circuits before fabrication. Since the device models provided by the foundry may not be accurate in the mmWave frequency band, separate test structures were implemented to determine the performance of the devices and components used in the phased array system. In this chapter, the modeling of active devices, vector modulator and balun are considered.

3.1 Measurement Procedure

All the device characterization and circuit measurements are done by on-wafer probing in a manual probe station. A block diagram of the measurement setup is shown below in Figure 8.

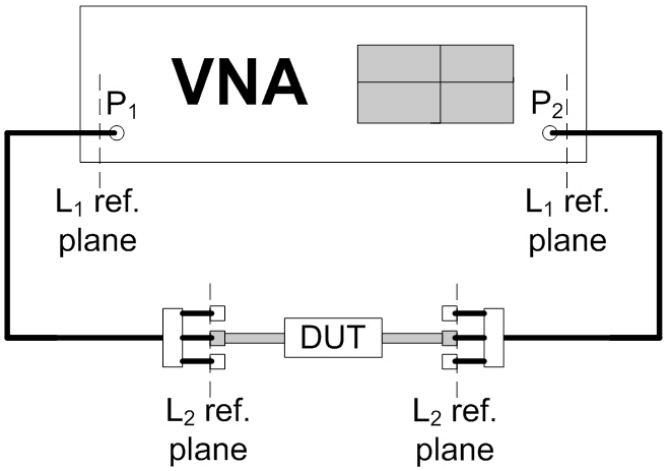


Figure 8: Measurement setup

The reference plane for the measurements is shifted from the VNA output (L_1) to the probe tips (L_2) by using LRRM calibration standard(using thru, open, short and load standard). After calibration, the only non-ideality in the measurement setup is the effect of GSG input/output pads on the measured component performance. To remove this effect, a separate test structure with back-to-back GSG pads is fabricated and measured. The

above measurement result can be used to determine the performance of a single GSG pad and, in turn, deembed the performance of the measured components from the calibrated measurement results.

3.2 Modeling of the Active device

A common source(CS) device forms the core of the active quadrature generator proposed later. Hence, a separate test structure is implemented for the CS device to determine its interface impedance and transfer characteristic accurately at mmWave frequency. The chip microphotograph of the fabricated active device is shown below in Figure 9.

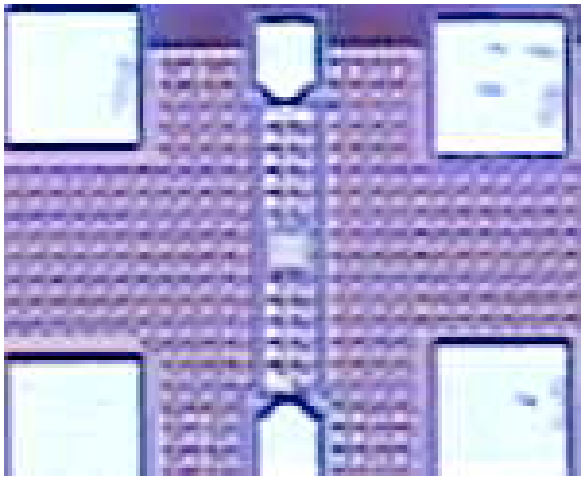


Figure 9: Chip microphotograph of active device

The parasitic model created for the active device using the measurement results is shown below in Figure 10.

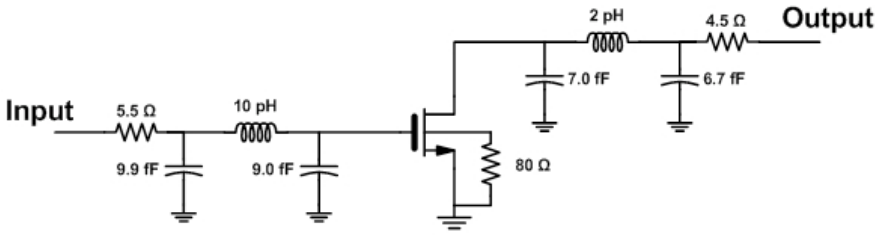
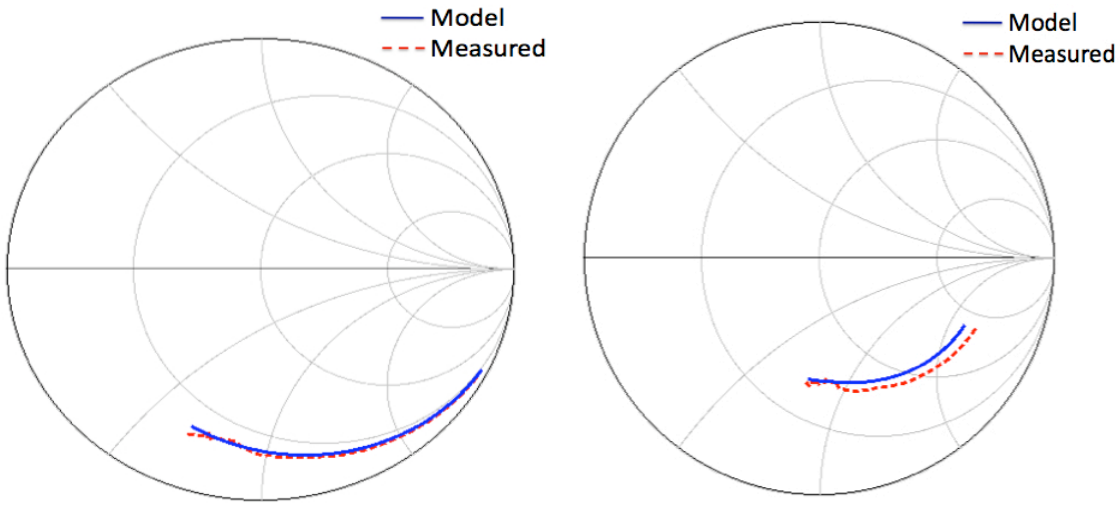


Figure 10: Parasitic model for the common source device

The input and output reflection coefficient of the measured device and the parasitic model created are shown below in Figure 11(a) and Figure 11(b).



(a) Input reflection coefficient(S_{11}) (b) Output reflection coefficient(S_{22})

Figure 11: Simulated and measured (a) Input reflection coefficient and (b) Output reflection coefficient of common source device

The S_{21} of the measured device and the parasitic model created are shown below in Figure 12. Here, we can see that the performance of the parasitic model is close to the measurement results. Hence, the created parasitic model can be used for predicting the performance of the active phase shifter accurately.

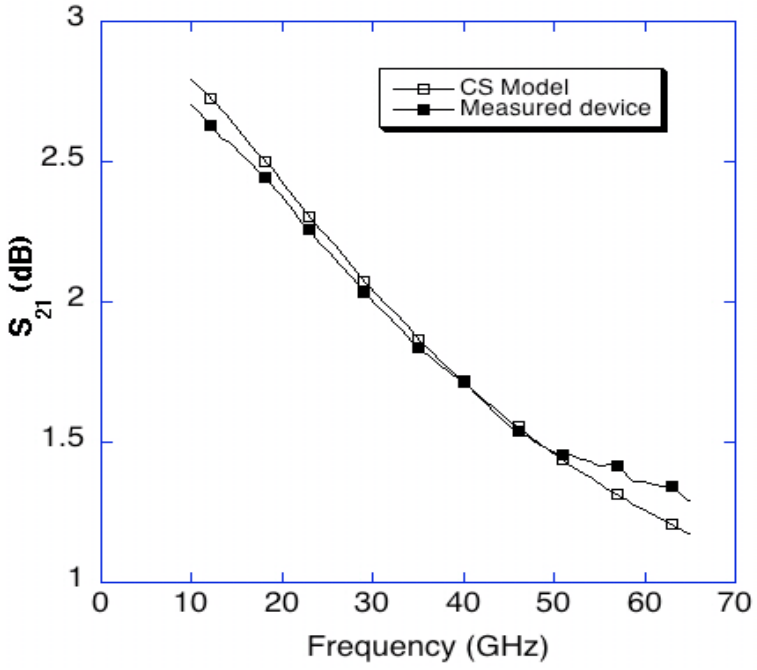


Figure 12: Simulated and measured S_{21} of common source device

3.3 Modeling of the Vector Modulator

The other important component used in the design of phase shifters is the weighed IQ summer (vector modulator). Hence, a vector modulator test structure is fabricated and measured to determine its interface impedances. The chip microphotograph of the fabricated vector modulator is shown below in Figure 13.

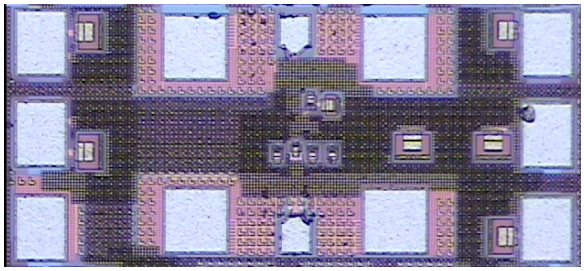


Figure 13: Chip microphotograph of the vector modulator

Two separate parasitic models are created for the vector modulator to match the measurement results. The first model uses the CC extracted view of the layout with the inclusion of some parasitic inductances at the interface terminals. The second parasitic model uses a more elaborate RLC structure with all the interconnect inductance, resistance and capacitance taken into consideration in the creation of the model. The RLC model created for the vector modulator is shown below in Figure 14.

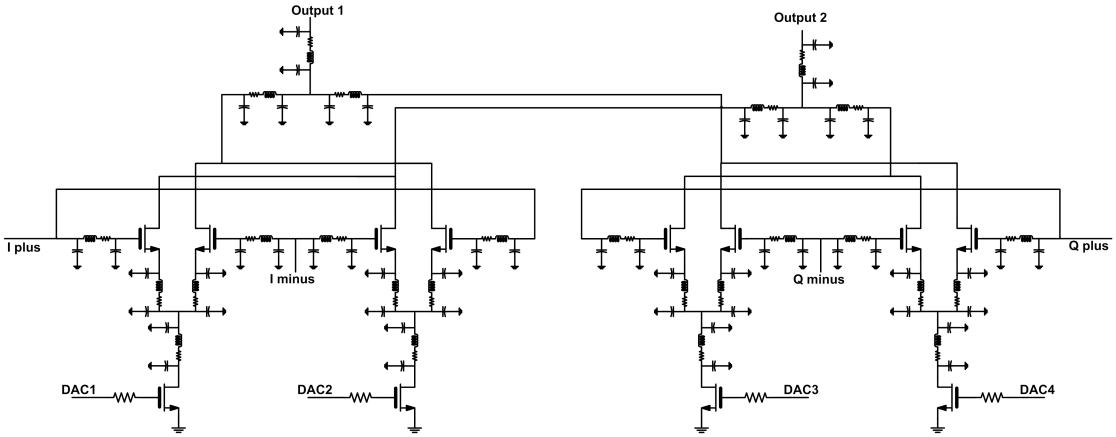
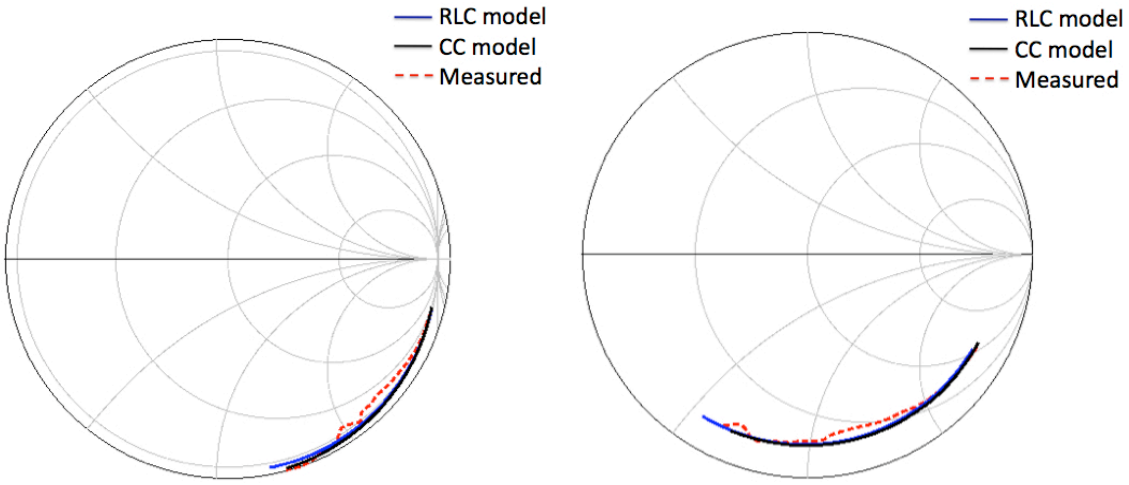


Figure 14: Parasitic model for the vector modulator

The input and output reflection coefficients of the measured vector modulator and the parasitic model created are shown below in Figure 15(a) and Figure 15(b).



(a) Input reflection coefficient(S_{11}) (b) Output reflection coefficient(S_{22})

Figure 15: Simulated and measured (a) Input reflection coefficient and (b) Output reflection coefficient of the vector modulator

One can see that the performance of the parasitic models is close to the measurement results. Hence, the created parasitic models can be used for predicting the performance of the phase shifters accurately. Also, the created RLC model is accurate in predicting the circuit performance. Hence, the RLC estimation technique can also be used to predict the performance of the components whose measurement results are not available.

3.4 Modeling of the Balun

To reduce die size and measurement complexity, the designed test structures have single-ended input/output feeding. But, the designed vector sum based active phase shifters operate only on differential signals. Hence, an on-chip marchand balun is used to generate differential signals from the single-ended input signal. The designed marchand balun consists of two coupled sections, each quarter wavelength long. The schematic of the designed balun is shown in Figure 16. To characterize the designed balun accurately in the frequency range(50GHz- 56GHz), a complete electromagnetic simulation is carried out.

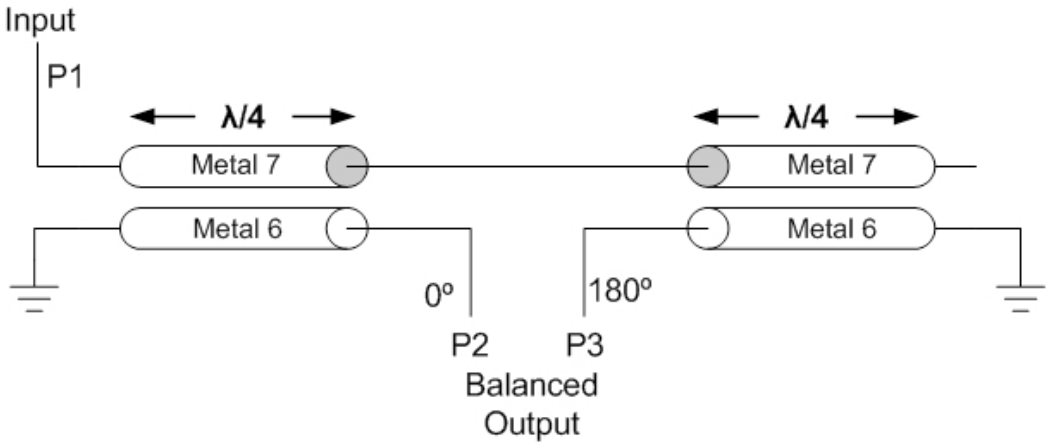


Figure 16: Schematic of the balun

The simulated input matching of the designed balun is shown below in Figure 17.

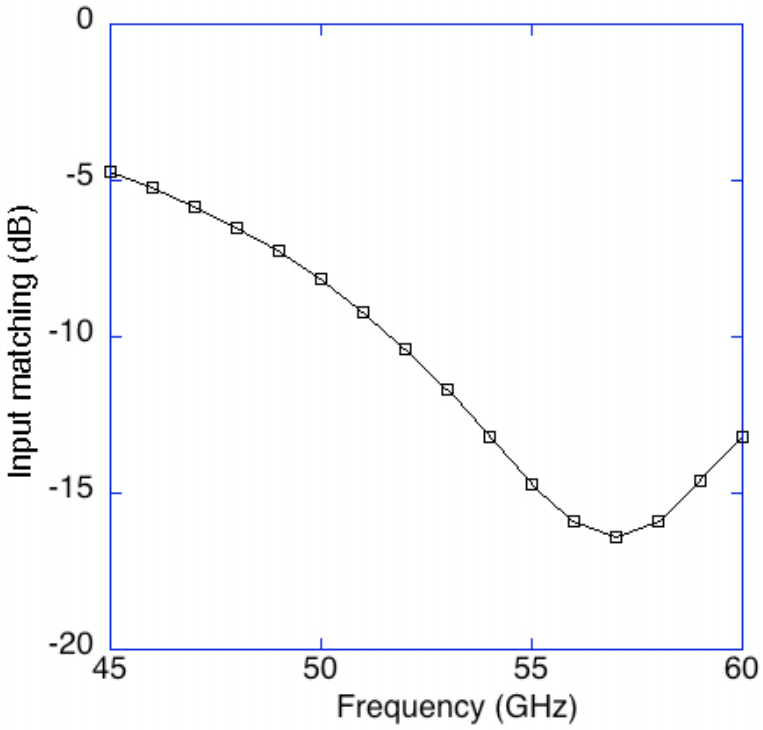


Figure 17: Input match of the balun

The simulated insertion loss and insertion phase of the designed balun are shown below in Figure 18 and Figure 19.

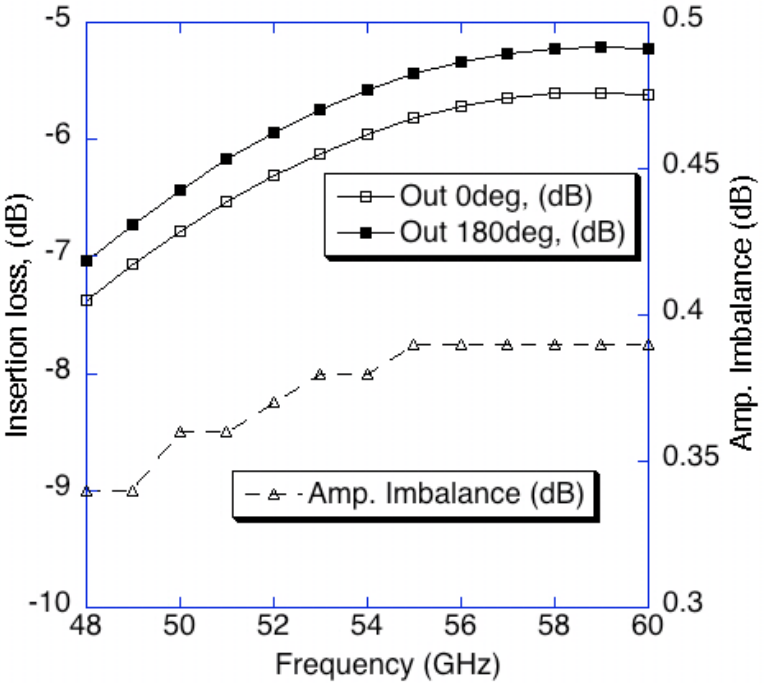


Figure 18: Insertion loss of the balun

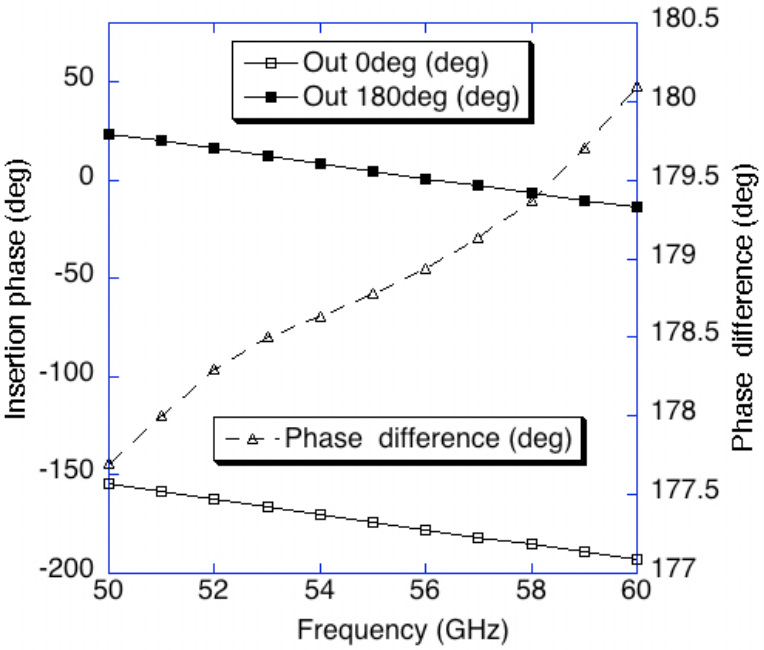


Figure 19: Insertion phase of the balun

CHAPTER IV

PASSIVE PHASE SHIFTER

4.1 Description

The passive phase shifters are the most common and widely used phase shifting architectures at lower mmWave frequencies. Simplicity, no DC power consumption and predictability of performance are some of the important advantages of a passive phase shifting architecture. But, these architectures suffer from higher insertion loss and inability to produce a continuous 360-degree phase shift. Some of the most common passive phase shifting architectures are given below.

- Reflection type phase shifter
- Switched line phase shifter
- Loaded line phase shifter
- Hybrid phase shifter

4.2 Design Procedure

The implemented passive phase shifter is based on the reflection type architecture. A coupled line section with tunable impedance networks as termination elements produce the required phase shift. The coupled section is designed to have a phase shift of 90 degrees at the center frequency of interest. By terminating the coupled section with variable impedance networks, the reflection and coupling between the input and output ports can be varied. This principle is used to vary the insertion phase of the designed passive phase shifter. The schematic of the passive phase shifter is shown below in Figure 20.

Since the performance of the passive phase shifter is highly dependant on the performance of the coupled sections and the matching networks, complete electromagnetic simulation is carried out using Agilent momentum and Zeland IE3D. The electromagnetic

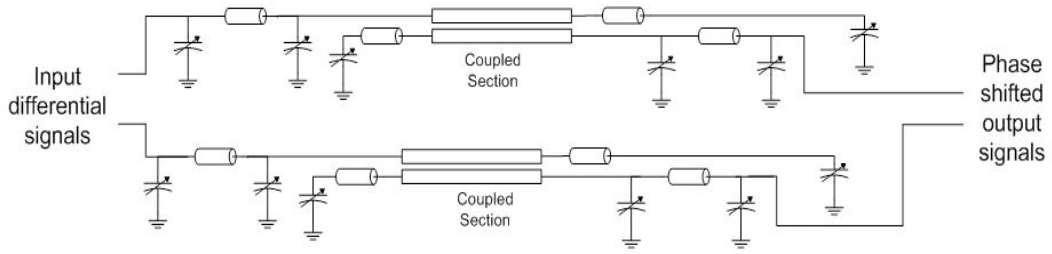


Figure 20: Schematic of passive phase shifter

simulation setup is shown below in Figure 21. The EM simulation results are used to tweak the circuit parameters to obtain the best possible system performances.

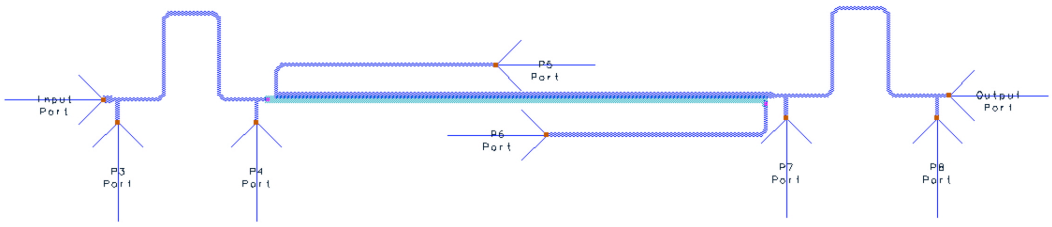


Figure 21: EM simulation setup for the passive phase shifter

4.3 Measurement Results

The chip microphotograph of the fabricated passive phase shifter is shown below in Figure 22.

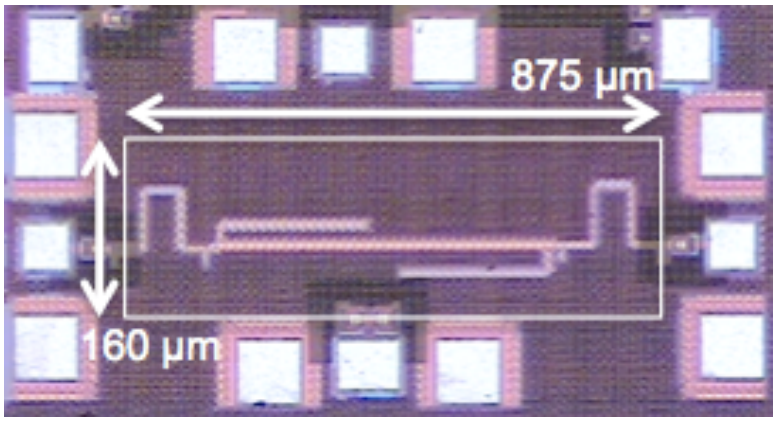


Figure 22: Chip microphotograph of the passive phase shifter

The simulated and measured input/output reflection coefficient of the passive phase shifter is shown below in Figure 23.

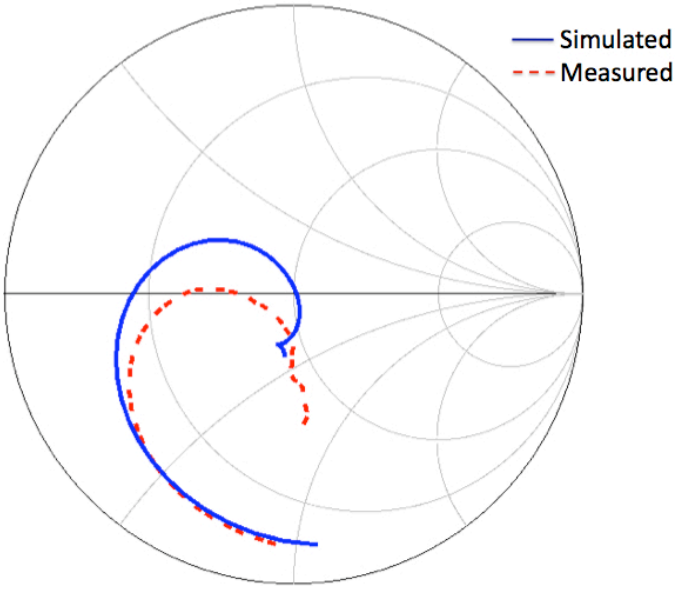


Figure 23: Simulated and measured input and output reflection coefficient

The measured insertion loss and phase shift variation with frequency for different phase shift control signals (Vctrl) are shown below in Figure 24 and Figure 25.

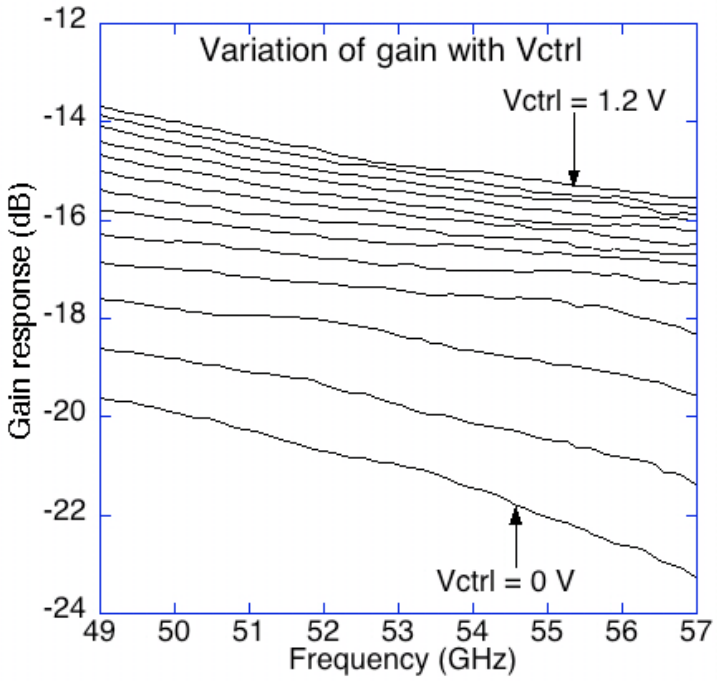


Figure 24: Measured amplitude variation for different control signals

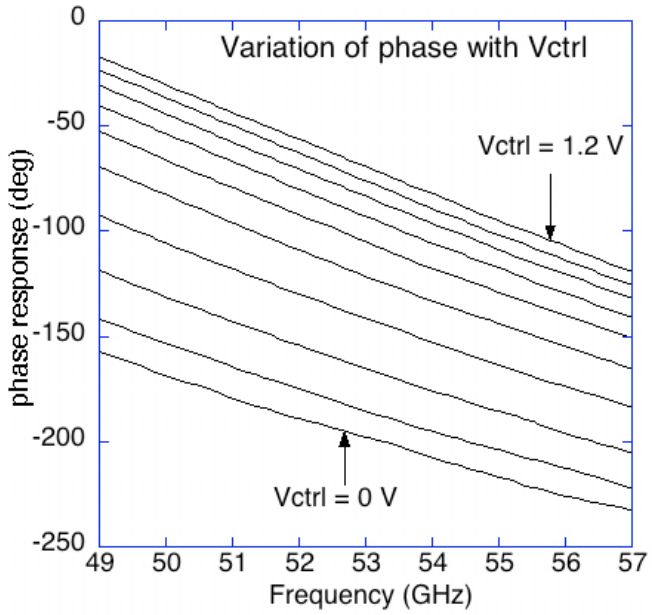


Figure 25: Measured phase shift variation for different control signals

The simulated and measured amplitude and phase shift variation for different phase shift control signals at 53GHz are shown below in Figure 26 and Figure 27. The measured average insertion loss and phase shift variation of the passive phase shifter are 16.75dB and 141^o respectively. These results are close to the simulated values of 13.5dB and 150^o.

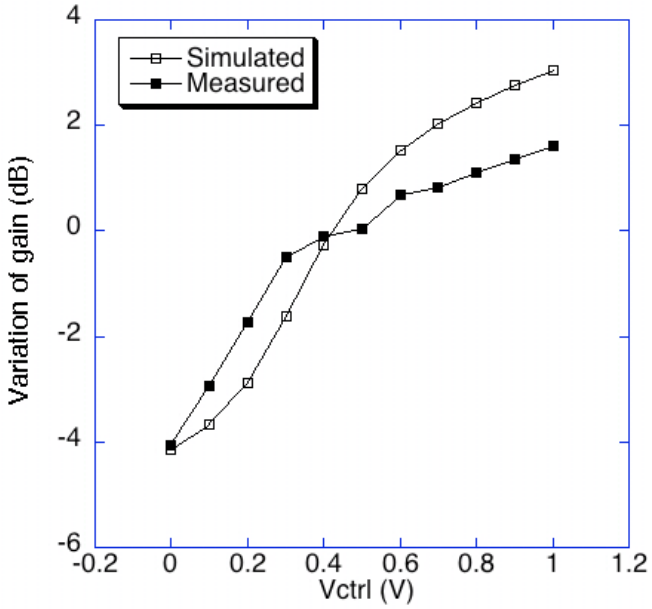


Figure 26: Simulated and measured amplitude variation for different control signals @ 53 GHz

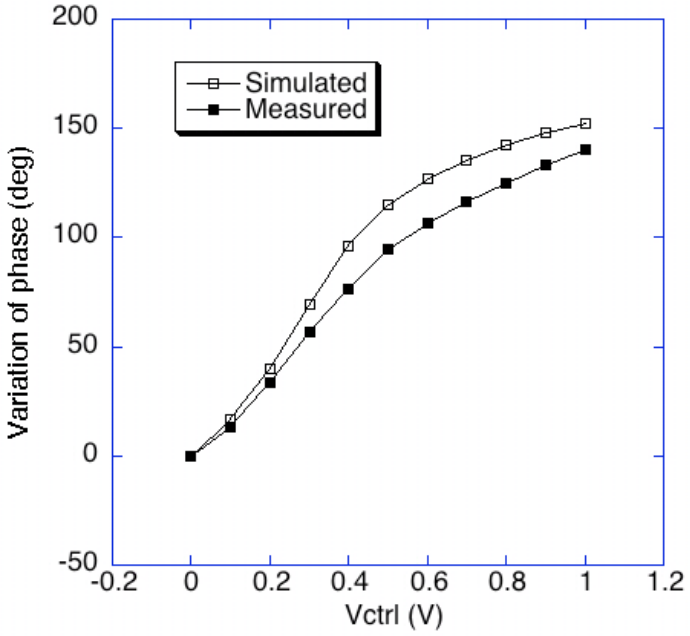


Figure 27: Simulated and measured phase shift variation for different control signals @ 53 GHz

The performance of the phase shifters can be quantified using their RMS gain error and RMS phase errors values [15] which are given by the following equations (11) and (12).

$$\theta_{\Delta,RMS} = \sqrt{\frac{1}{N-1}\sum_{i=2}^{N}|\theta_{\Delta i}|^2} \tag{11}$$

$$A_{\Delta,RMS} = \sqrt{\frac{1}{N}\sum_{i=1}^{N}|A_{\Delta i}|^2} \tag{12}$$

where $A_{\Delta i} = A_{vi}$ - $A_{average}$ and $\theta_{\Delta i}$ = ith output phase error from ideal phase value

The obtained RMS gain error of the passive phase shifter is shown below in Figure 28.

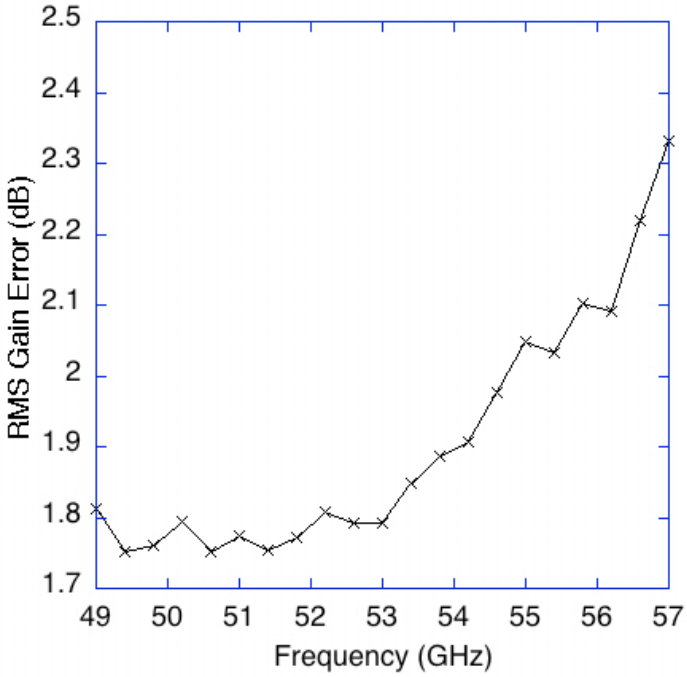


Figure 28: Variation of RMS gain error with frequency

4.4 Performance Summary

The performance summary of the passive phase shifter is shown below in Table 2

Table 2: Performance of the passive phase shifter

Performance parameter	**Measured Result**
Frequency (GHz)	50-56
Average Gain (dB)	-16.75
RMS Gain error (dB)	<2.1
Phase Shift Range(^{o})	141
Area (mm^2)	0.14
Power (mW)	0
Technology	90nm CMOS

From the above performance summary, it is clear that the passive phase shifter is an excellent candidate for ultra low power compact phased array system implementations.

CHAPTER V

PASSIVE QUADRATURE GENERATOR BASED ACTIVE PHASE SHIFTER

5.1 Description

Passive phase shifters are excellent candidates for ultra low power compact phased array systems. However, most of the passive phase shifters cannot produce phase shift across the entire 360 degree range with acceptable insertion loss and RMS gain error. A vector modulator based phase shifter, which consists of a quadrature generator followed by a vector modulator, can be used to produce a continuous 360^o phase shift range with acceptable gain variation. The quadrature generator is used to produce the quadrature differential signals from the input differential signals, while the vector modulator is used to perform weighed IQ summing to produce the required phase shift. A block diagram of the vector modulator based phase shifter is shown below in Figure 29.

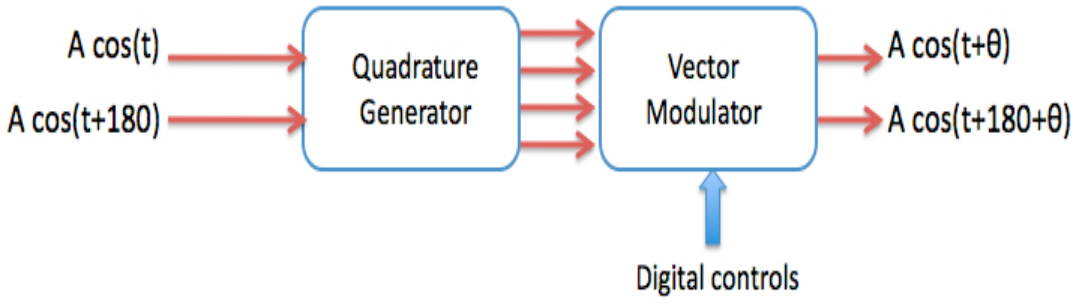


Figure 29: Block diagram of vector modulator based phase shifter

A detailed circuit diagram of the vector modulator(VM) is shown below in Figure 30.

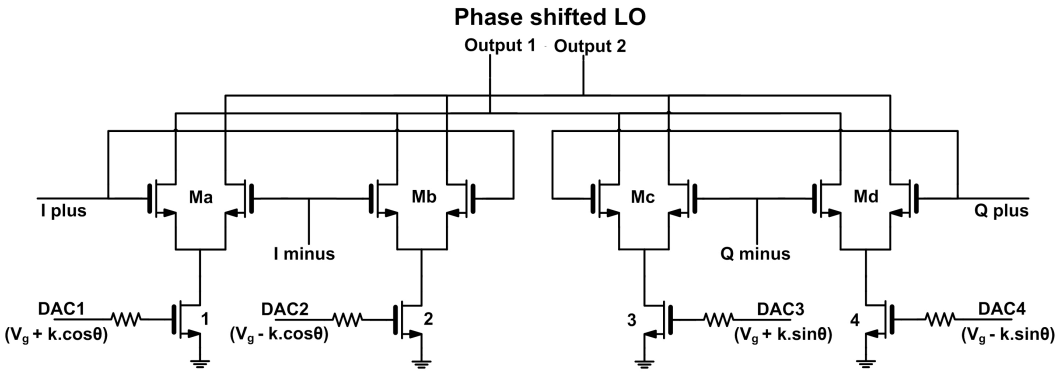


Figure 30: Schematic of the active vector modulator

The circuit operation of the vector modulator can be explained mathematically by assuming that all the devices follow square law behavior (i.e) $I_d \propto (V_{gs})^2$. The current through the devices M_1, M_2, M_3, M_4 can be written as follows.

$$\begin{aligned} I_1 &\propto (V_g + k.\cos\theta)^2 \\ I_2 &\propto (V_g - k.\cos\theta)^2 \\ I_3 &\propto (V_g + k.\sin\theta)^2 \\ I_4 &\propto (V_g - k.\sin\theta)^2 \end{aligned}$$

Under small signal conditions,

$$\begin{aligned} i_{Ma} &= Gm_{Ma}.LO_I \\ i_{Mb} &= -Gm_{Mb}.LO_I \\ i_{Mc} &= Gm_{Mc}.LO_Q \\ i_{Md} &= -Gm_{Md}.LO_Q \end{aligned}$$

where $Gm_{a,b,c,d} \propto I^{0.5}$

The relationship between the output current and the branch currents is given below.

$$\begin{aligned} i_{out1} &= i_{Ma} + i_{Mb} + i_{Mc} + i_{Md} \\ &= Gm_{Ma}.LO_I - Gm_{Mb}.LO_I + Gm_{Mc}.LO_Q - Gm_{Md}.LO_Q \\ &\propto (V_g + k.\cos\theta).LO_I - (V_g - k.\cos\theta).LO_I + (V_g + k.\sin\theta).LO_Q - (V_g - k.\sin\theta).LO_Q \end{aligned}$$

Since the quadrature LO signals have some amplitude imbalance, ΔA and phase imbalance, $\Delta\phi$, the input LO signals can be written as follows:

$$LO_I = (A + \Delta A/2) \,.\, \cos(wt + \Delta\phi/2)$$

$$\overline{LO_I} = -\,(A + \Delta A/2) \,.\, \cos(wt + \Delta\phi/2)$$

$$LO_Q = (A - \Delta A/2) \,.\, \sin(wt - \Delta\phi/2)$$

$$\overline{LO_Q} = -\,(A - \Delta A/2) \,.\, \sin(wt - \Delta\phi/2)$$

Therefore,

$$i_{out1} \quad \propto \quad k.\cos\theta.\,(A + \Delta A/2) \,.\, \cos(wt + \Delta\phi/2) + k.\sin\theta.\,(A - \Delta A/2) \,.\, \sin(wt - \Delta\phi/2)$$

$$i_{out1} \quad \propto \quad k.A.\cos(wt - \theta) \qquad\qquad [In\ ideal\ case,\ \Delta A = 0,\ \Delta\phi = 0]$$

From the above equation, it is evident that the vector modulator can be used as a LO phase shifter by applying proper control signals.

The quadrature generator used in a VM based active phase shifter can be implemented using either passive or active components. The schematic of the passive quadrature generation based active phase shifter is shown below in Figure 31.

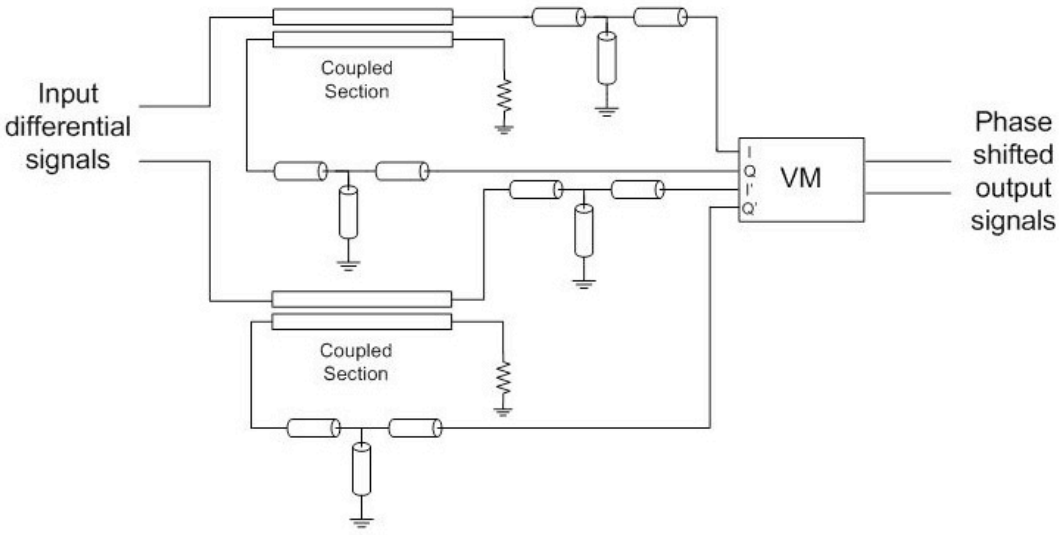


Figure 31: Schematic of the passive quadrature generator based active phase shifter

5.2 Design Procedure

The passive quadrature generator is implemented using a parallel-coupled section. The length and the coupling co-efficient between the two parallel lines determine the phase difference that can be obtained between the two output arms. If the coupled line section is designed to be quarter wavelength long at the design frequency (53GHz), the s-parameter matrix for the 4 port coupled line section [1] is given as

$$S_{para} = \begin{vmatrix} 0 & C & -j\sqrt{1-C^2} & 0 \\ C & 0 & 0 & -j\sqrt{1-C^2} \\ -j\sqrt{1-C^2} & 0 & 0 & C \\ 0 & -j\sqrt{1-C^2} & C & 0 \end{vmatrix}$$

If the coupling co-efficient, $C = \frac{1}{\sqrt{2}}$, the above s-parameter matrix can be rewritten as

$$S_{para} = \begin{vmatrix} 0 & \frac{1}{\sqrt{2}} & \frac{-j}{\sqrt{2}} & 0 \\ \frac{1}{\sqrt{2}} & 0 & 0 & \frac{-j}{\sqrt{2}} \\ \frac{-j}{\sqrt{2}} & 0 & 0 & \frac{1}{\sqrt{2}} \\ 0 & \frac{-j}{\sqrt{2}} & \frac{1}{\sqrt{2}} & 0 \end{vmatrix}$$

In the above s-parameter matrix, the insertion phase difference between the output ports 2 and 3 is 90^o. This relationship is valid only for a 50-ohm termination impedance. Hence, a symmetric matching network is used to transform the VM input impedance to 50 ohms. Also, the symmetric matching network preserves the quadrature phase shift between the output terminals. A complete EM simulation is carried out using Agilent momentum and Zeland IE3D for the passive quadrature generator based active phase shifter to include all the layout non-idealities. The EM simulation setup for the passive quadrature generator based active phase shifter is shown below in Figure 32. The obtained EM simulation results are used to tweak the system performance.

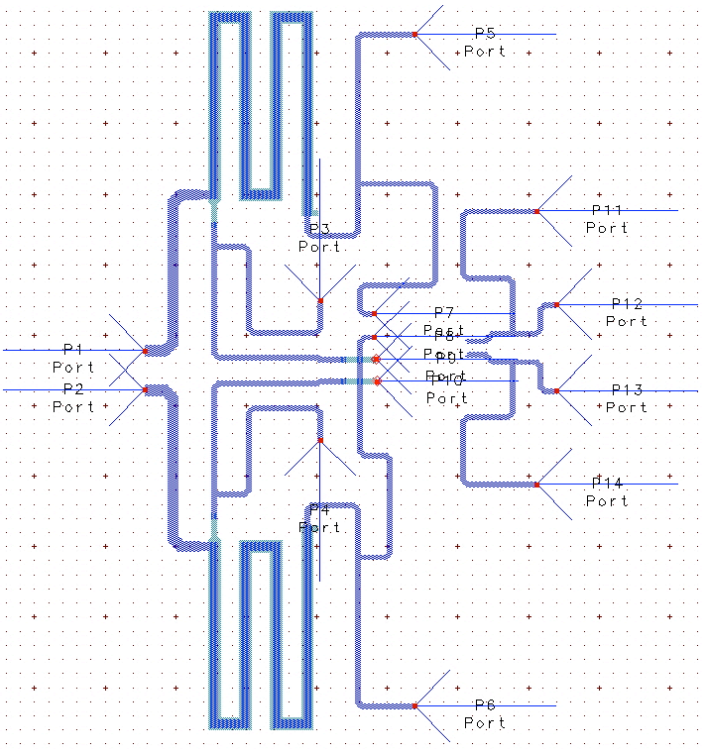


Figure 32: EM simulation setup for the passive quadrature generator based active phase shifter

5.3 Measurement Results

The chip microphotograph of the fabricated passive quadrature generator based active phase shifter is shown below in Figure 33.

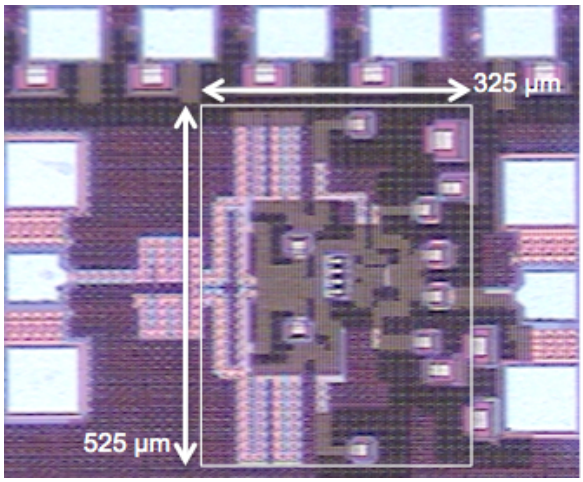


Figure 33: Chip microphotograph of the passive quadrature generator based active phase shifter

The simulated and measured input and output reflection coefficients of the passive quadrature generator based active phase shifter are shown below in Figure 34 and Figure 35.

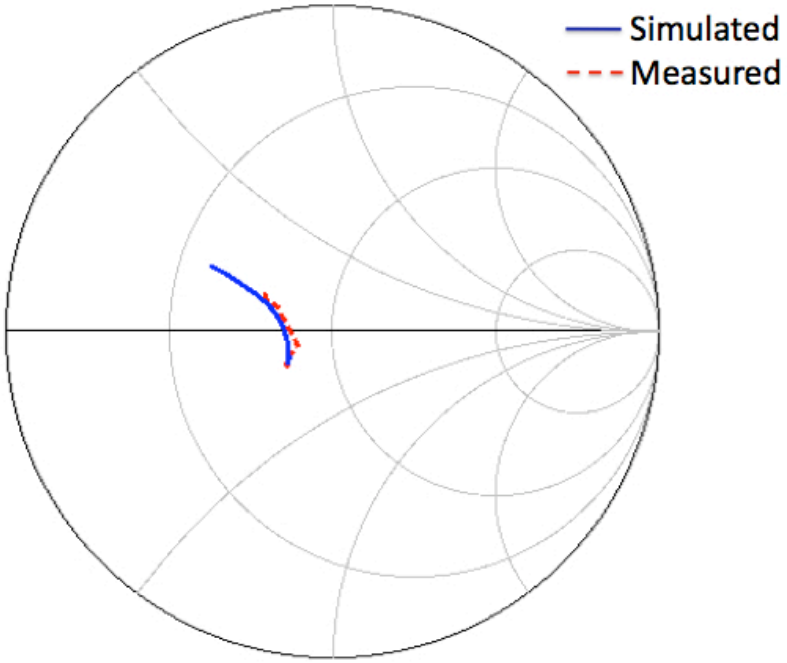


Figure 34: Simulated and measured input reflection coefficient

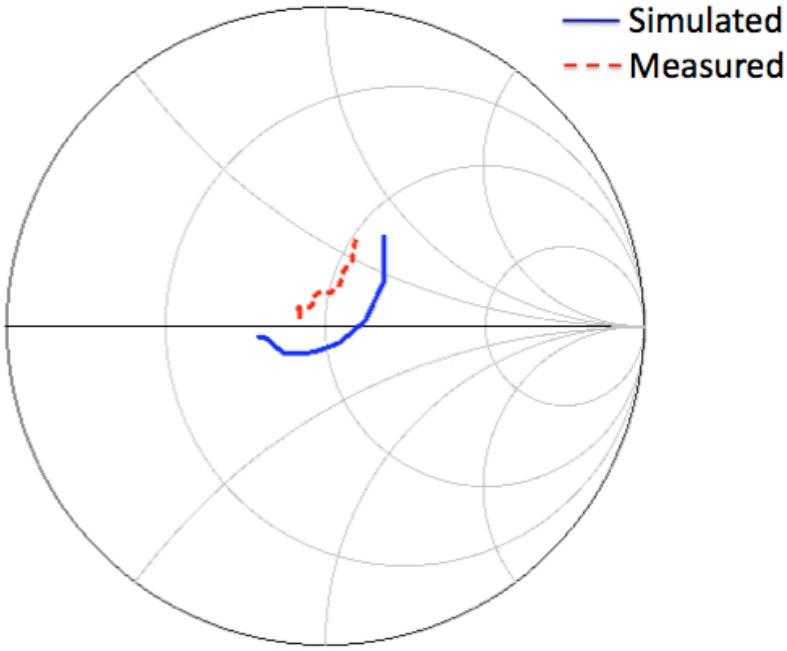


Figure 35: Simulated and measured output reflection coefficient

Due to some modeling issues in the coupled section, there is a slight up shift in the frequency response of the passive quadrature generator based active phase shifter. Hence, the measured results have better performance in the frequency range from 54GHz to 60GHz compared to the target 50GHz-56GHz range.

Since the passive quadrature generator output is matched to the VM input, the performance of the passive quadrature generator cannot be measured directly. The amplitude balance and phase accuracy of the quadrature generator can be measured indirectly by setting DAC_1=400mV, $DAC_{2,3,4}$=0 to determine the performance of in-phase signal and DAC_4=400mV, $DAC_{1,2,3}$=0 to determine the performance of quadrature signal. The obtained results are tabulated below in Table 3.

Table 3: Performance of the passive quadrature generator

Performance parameter	**Measured**				
Frequency(GHz)	50	53	56	59	62
Amplitude Imbalance (dB)	2.5	1.8	1	1.3	1.8
Phase Imbalance (^{o})	30	20	18	7	11

The measured insertion loss and phase shift variation with frequency for different phase shift control signals are shown below in Figure 36 and Figure 37.

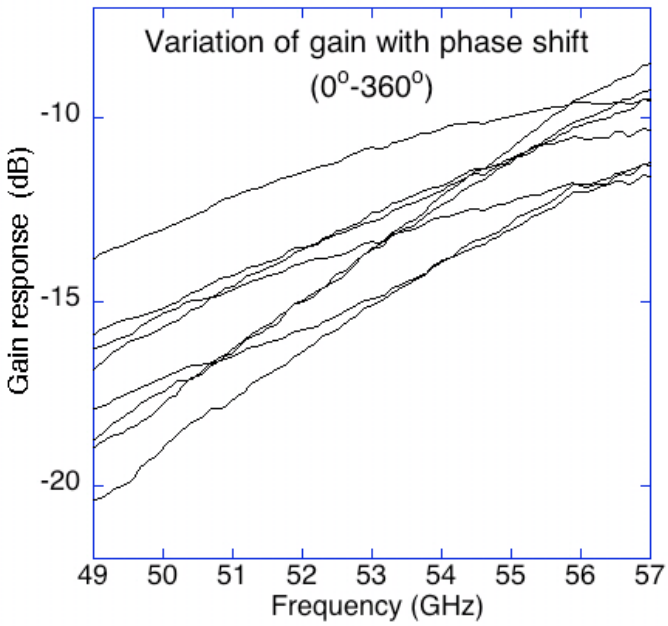


Figure 36: Measured amplitude variation for different control signals

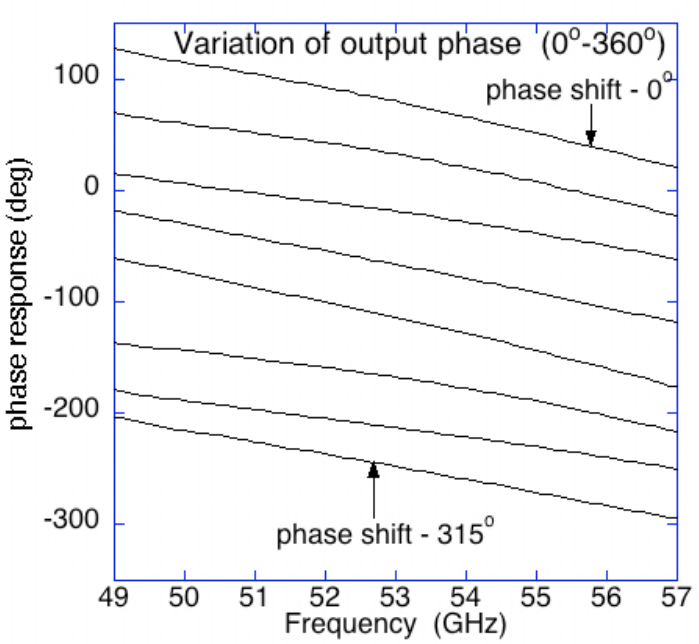


Figure 37: Measured phase shift variation for different control signals

The simulated and measured amplitude variation(wrt mean) and phase shift variation for different phase shift control signals at 56GHz are shown below in Figure 38 and Figure 39. The measured and simulated average insertion loss of the phase shifter are 13.5dB and 8dB respectively.

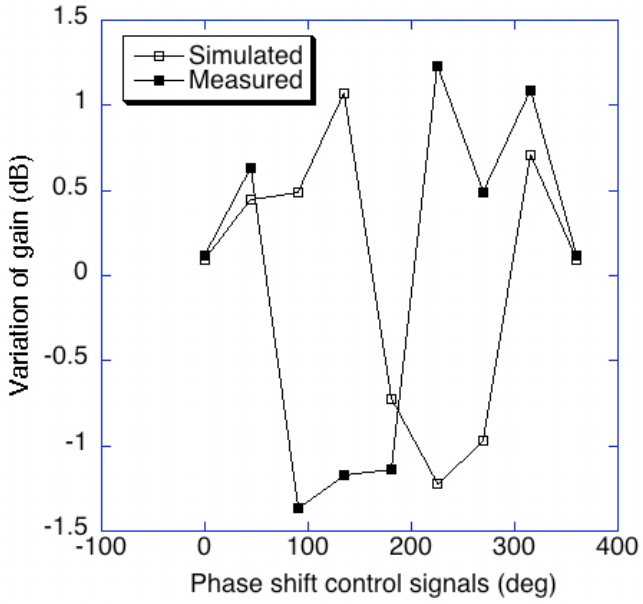


Figure 38: Simulated and measured amplitude variation for different control signals @ 56GHz

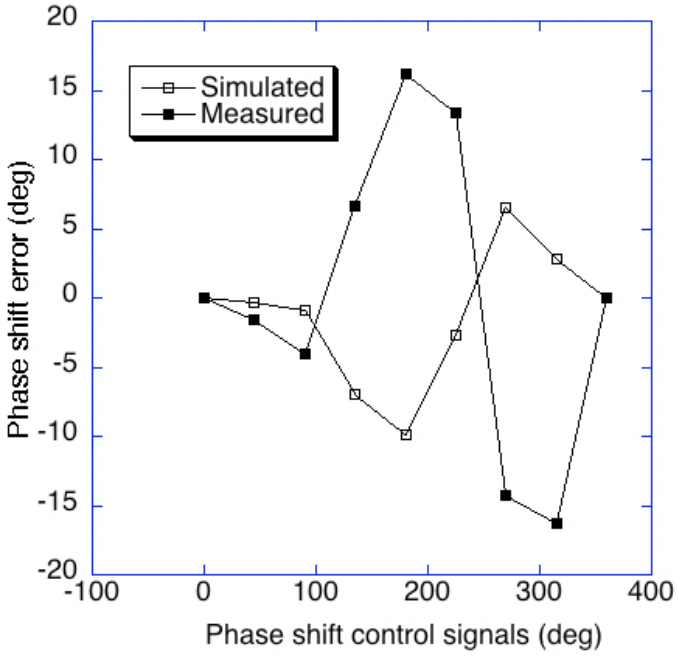


Figure 39: Simulated and measured phase shift variation for different control signals @ 56GHz

The RMS gain error and phase error of the passive quadrature generator based active phase shifter are determined using equations (11) and (12). The variation of these parameters with frequency is shown below in Figure 40 and Figure 41.

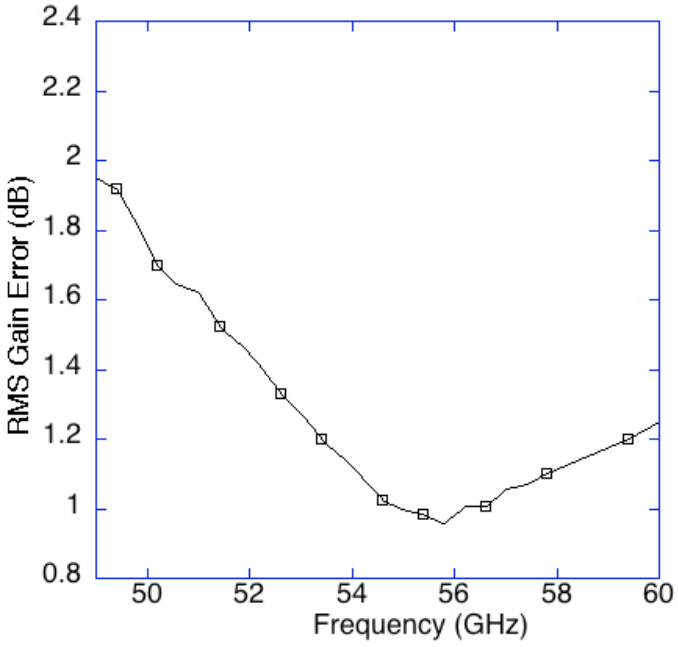


Figure 40: Variation of RMS gain error with frequency

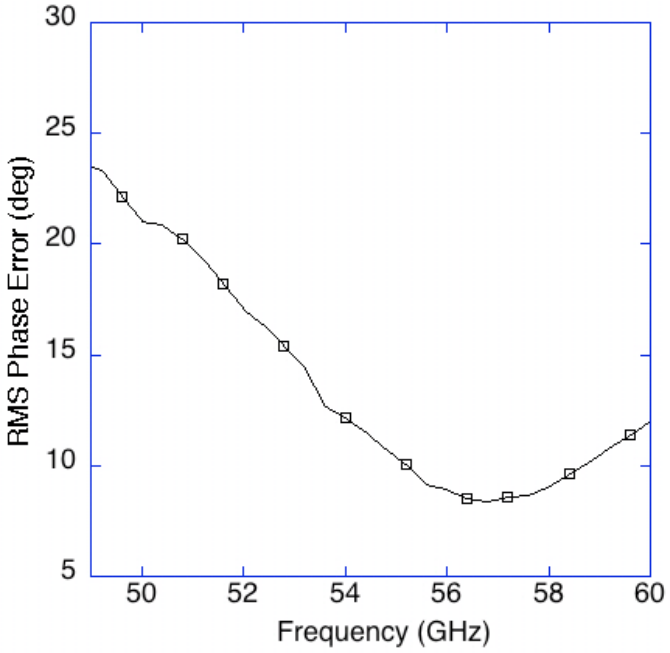


Figure 41: Variation of RMS phase error with frequency

5.4 Performance Summary

The complete performance summary of the passive quadrature generator based active phase shifter is shown below in Table 4.

Table 4: Performance of the passive quadrature generator based active phase shifter

Performance parameter	**Measured Result**	
Frequency (GHz)	50-56	54-60
Average Gain (dB)	-13.5	-11
RMS Gain error (dB)	<1.76	<1.25
RMS Phase error (^{o})	<21	<12
Phase Shift Range(^{o})	360	
Area (mm^2)	0.17	
Power (mW)	6	
Technology	90nm CMOS	

CHAPTER VI

ACTIVE QUADRATURE GENERATOR BASED ACTIVE PHASE SHIFTER

6.1 Description

The passive phase shifter and the passive quadrature generator based active phase shifter have high insertion loss at mmWave frequency. To overcome this issue, a novel active quadrature generation circuitry and an active quadrature generator based active phase shifter are proposed [30]. Due to the presence of active devices in the quadrature generation circuitry, the proposed architecture has smaller insertion loss compared to other circuits discussed. A schematic of the active quadrature generator based active phase shifter is shown below in Figure 42.

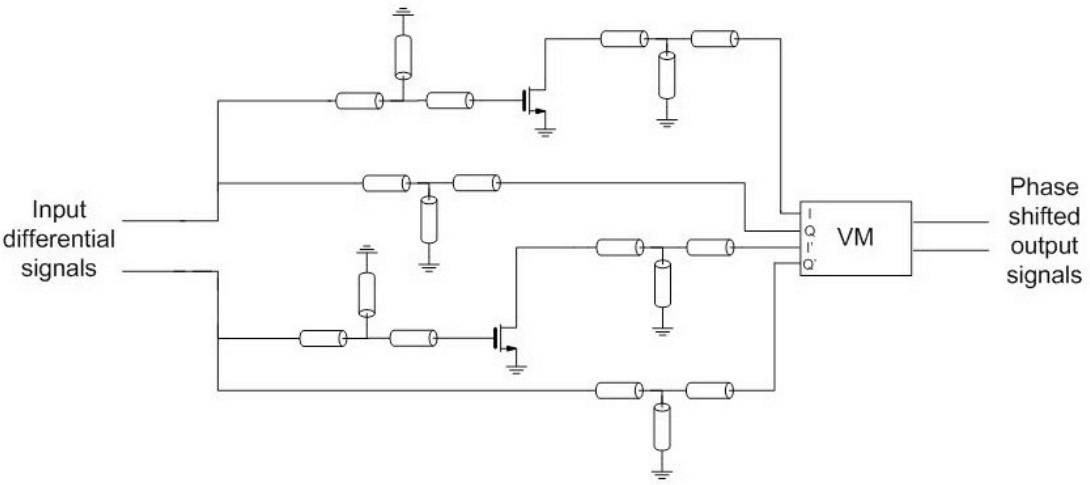


Figure 42: Schematic of the active quadrature generator based active phase shifter

6.2 Design Procedure

The proposed novel active quadrature generator uses an active device to produce the required phase shift. The complete design procedure for the active quadrature generator is given below.

- Modeling of devices

  Since the performance of the active quadrature generator depends on the performance (interface impedance and insertion loss) of the active device and the VM, separate test structures were implemented to determine their performances accurately. (Refer Chapter 3)

- Design of matching networks

  Here, T-matching networks are used to transform the active device input impedance to 50 ohms and for inter stage matching between the active device output and the vector modulator input. At mmWave frequency, the gain and the phase shift produced by an active device depends on the impedance presented at the source and the drain terminals of the common source device. Hence, the input and output matching networks were designed to produce optimum overall gain and quadrature phase relationship at the vector modulator inputs(I and Q).

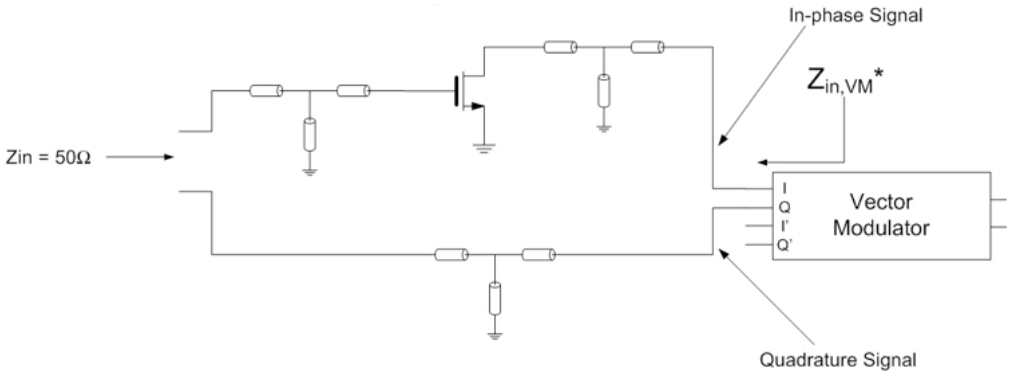


Figure 43: Schematic of the active quadrature generator

A complete EM simulation is carried out using Agilent momentum and Zeland IE3D for the active quadrature generator based active phase shifter to include all the layout non-idealities. The EM simulation setup for the active quadrature generator based active phase

shifter is shown below in Figure 44. The obtained EM simulation results are used to tweak the system performances.

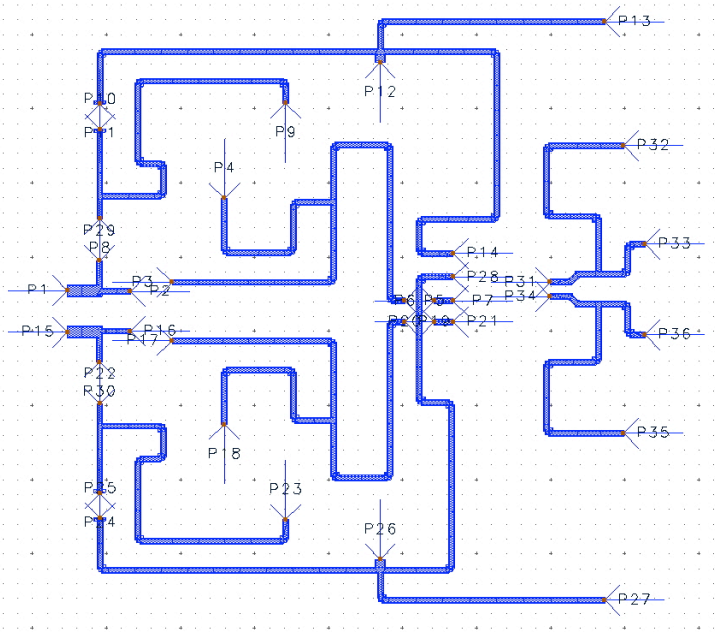


Figure 44: EM simulation setup for the active quadrature generator based active phase shifter

6.3 Measurement Results

The chip microphotograph of the fabricated active quadrature generator based active phase shifter is shown below in Figure 45.

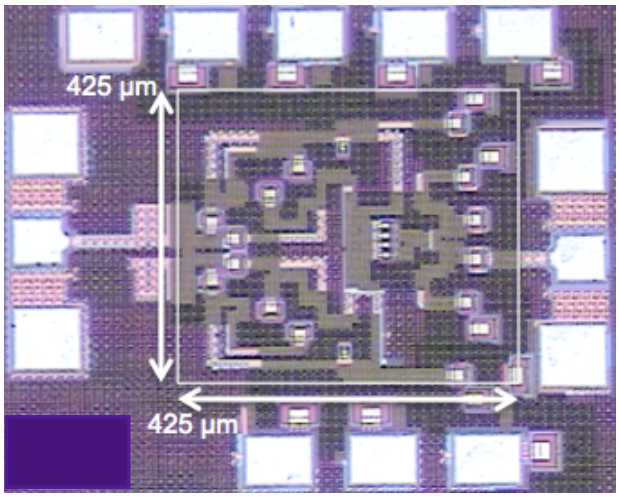


Figure 45: Chip microphotograph of active quadrature generator based active phase shifter

The simulated and measured input reflection coefficient of the active quadrature generator based active phase shifter are shown below in Figure 46.

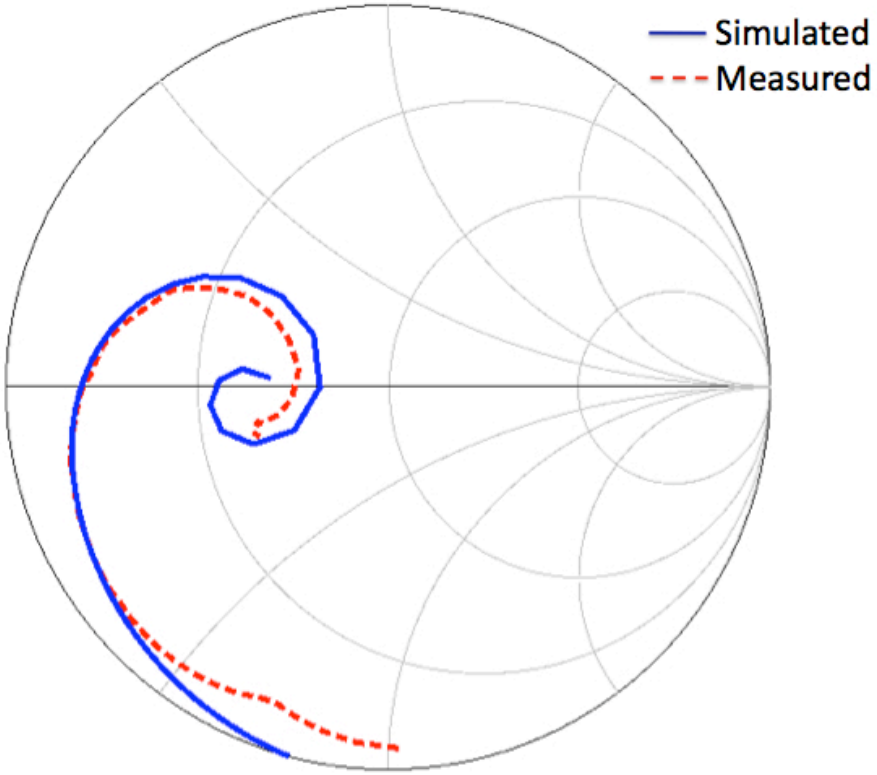


Figure 46: Simulated and measured input reflection coefficient

Since the active quadrature generator output is matched to the VM input, the performance of the active quadrature generator cannot be measured directly. The amplitude balance and phase accuracy of the quadrature generator can be measured indirectly by setting DAC_1=400mV, $DAC_{2,3,4}$=0 to determine the performance of in-phase signal and DAC_4=400mV, $DAC_{1,2,3}$=0 to determine the performance of quadrature signal. The results obtained using the above procedure are tabulated below in Table 5.

Table 5: Performance of the active quadrature generator

Performance parameter	**Simulated**			**Measured**		
Frequency(GHz)	50	53	56	50	53	56
Amplitude Imbalance (dB)	1.2	0.3	1.2	1.9	1	0.9
Phase Imbalance (^{o})	5	4	8	8	4	5

The simulated and measured insertion loss and phase shift variation with frequency for different phase shift control signals are shown below in Figure 47 and Figure 48.

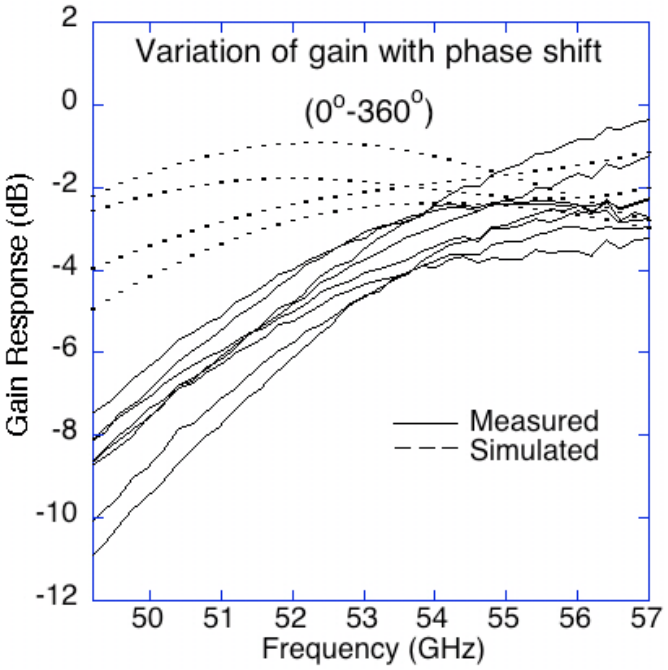


Figure 47: Simulated and measured amplitude variation for different control signals

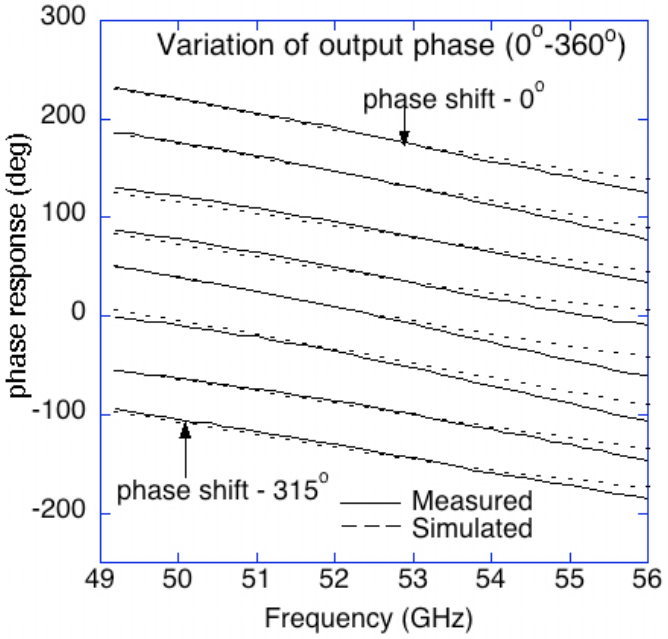


Figure 48: Simulated and measured phase shift variation for different control signals

The simulated and measured amplitude variation(wrt mean) and phase shift variation for different phase shift control signals at 53GHz are shown below in Figure 49 and Figure 50. The simulated and measured average insertion loss of the phase shifter are 2.8dB and 4.9dB respectively.

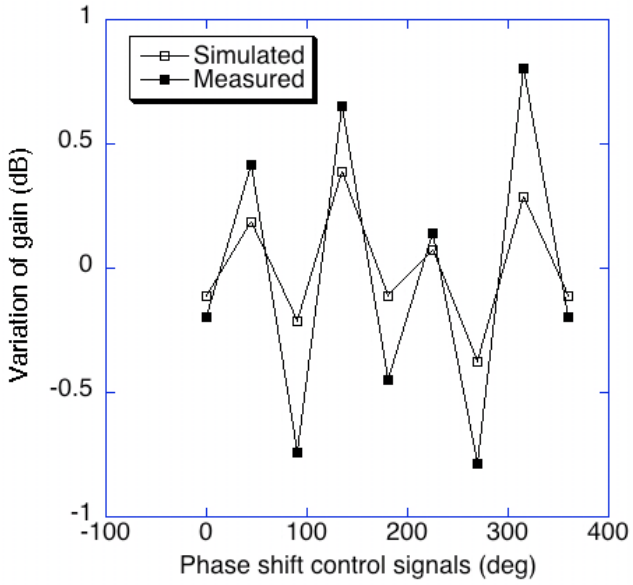


Figure 49: Simulated and measured amplitude variation for different control signals @ 53 GHz

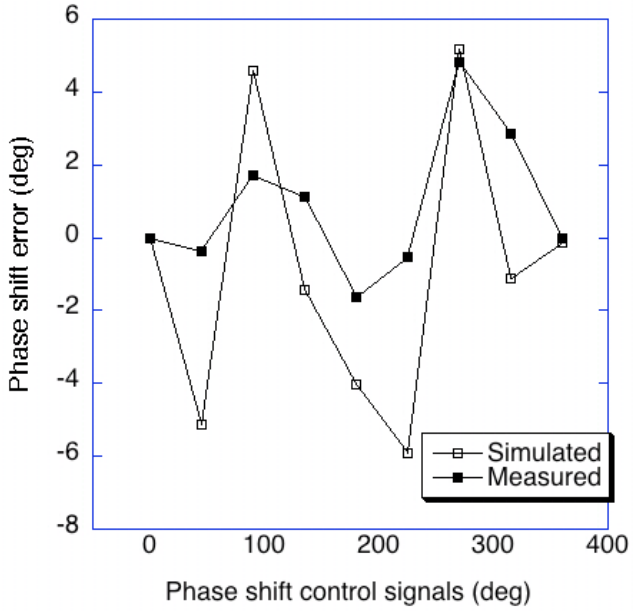


Figure 50: Simulated and measured phase shift variation for different control signals @ 53 GHz

The RMS gain error and RMS phase error of the active quadrature generator based active phase shifter are determined using equations (11) and (12). The variation of these parameters with frequency are shown below in Figure 51 and Figure 52

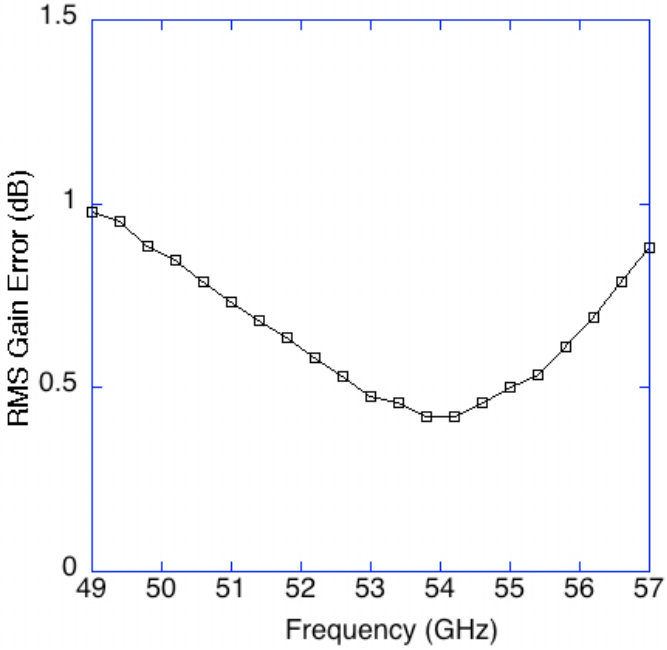


Figure 51: Variation of RMS gain error with frequency

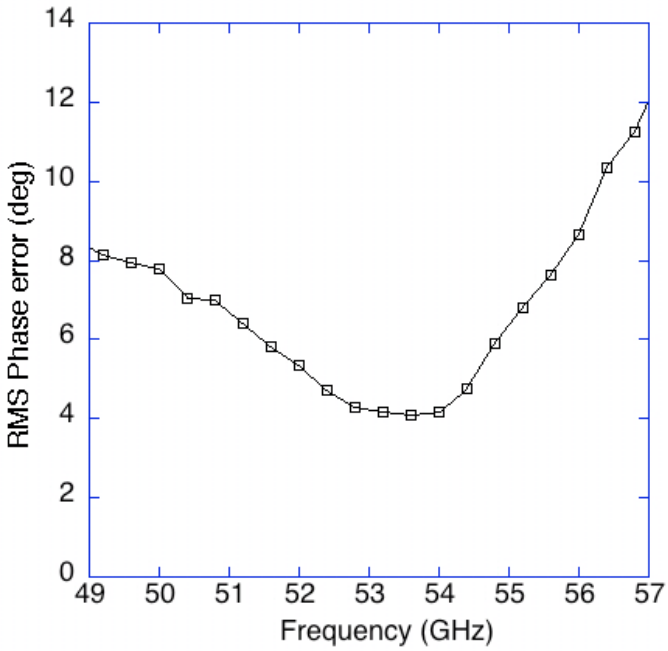


Figure 52: Variation of RMS phase error with frequency

Apart from phase shifting, the active quadrature generator based active phase shifter can also be used for direct up conversion of QPSK and n-QAM signals in a transmitter. In these systems, the DAC control signals are replaced by the required data signals that need to be up converted. The static output constellation for a QPSK input signal is shown below in Figure 53.

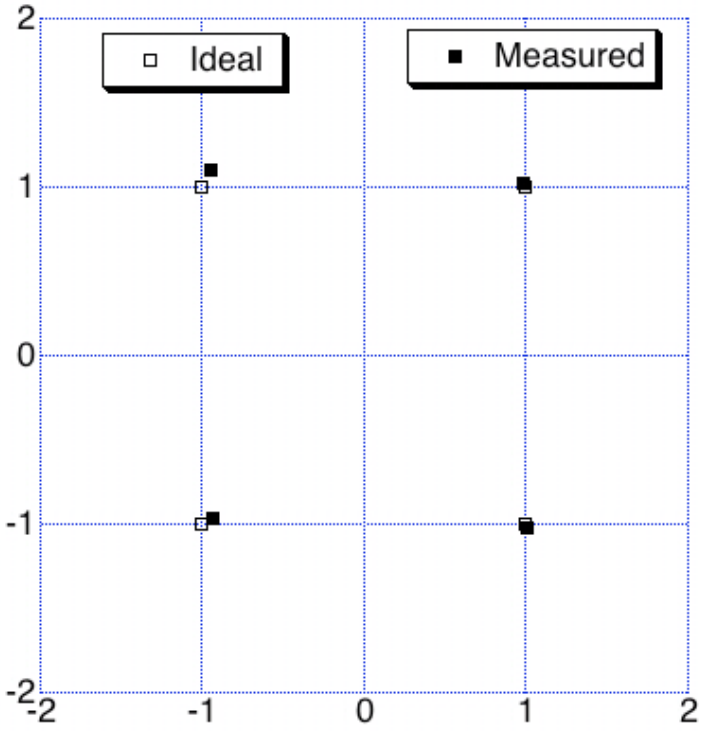


Figure 53: Ideal and measured output QPSK constellation @ 53GHz

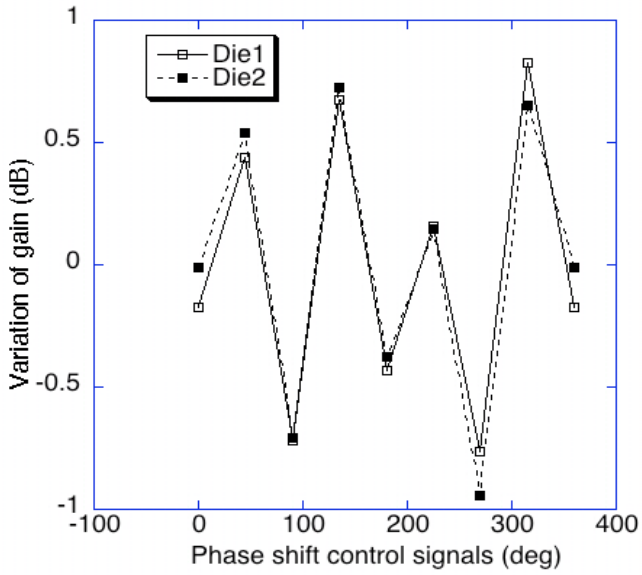
Table 6: Output QPSK constellation

Ideal		**Measured**	
Amp.	Phase	Amp.	Phase
1.414	45	1.421	46.0
1.414	135	1.457	130.5
1.414	225	1.344	225.7
1.414	315	1.435	314.3

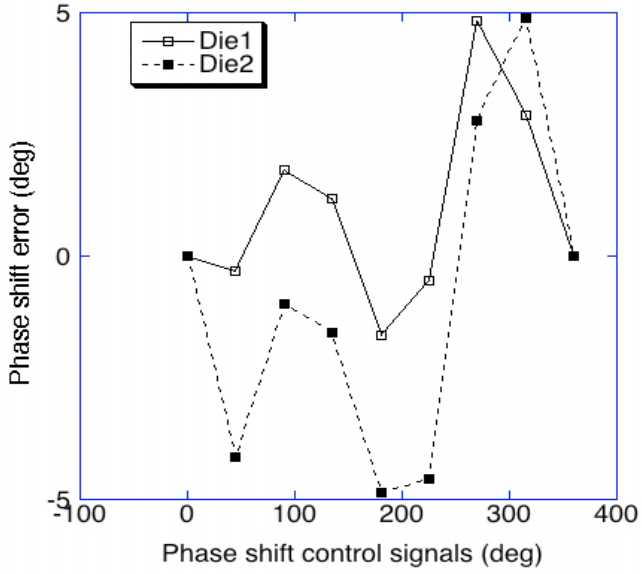
The EVM of the measured output constellation is 5.1%.

$$EVM = \sqrt{\frac{\frac{1}{N}\sum_{k=1}^{N}\left[(I_{k,ideal} - I_{k,actual})^2 + (Q_{k,ideal} - Q_{k,actual})^2\right]}{\frac{1}{N}\sum_{k=1}^{N}\left[I_{k,ideal}^2 + Q_{k,ideal}^2\right]}} \; X \; 100 \quad \% \qquad (13)$$

The gain and phase shift performance of the active quadrature generator based active phase shifter are measured for two arbitrary chips and the obtained results are shown below in Figure 54(a) and Figure 54(b). From the results, it is clear that the performance of the circuit doesn't vary from die-to-die.



(a) Gain variation



(b) Phase shift variation

Figure 54: Measured (a) gain variation and (b) phase shift variation for different control signals @ 53 GHz

6.4 Performance Summary

The complete performance summary of the active quadrature generator based active phase shifter is shown below in Table 7. The designed structure has superior performance in a narrower band (53GHz-54GHz) as tabulated below.

Table 7: Performance of the active quadrature generator based active phase shifter

Performance parameter	**Measured Result**	
Frequency (GHz)	50-56	53-54
Average Gain (dB)	-4.9	-4
RMS Gain error (dB)	<0.86	<0.42
RMS Phase error (^{o})	<8.64	<4.2
Phase Shift Range(^{o})	360	
Area (mm^2)	0.18	
Power (mW)	23	
Technology	90nm CMOS	

6.5 Comparison with Existing Work

The performance of the different phase shifters designed are tabulated and compared with the other reported works in Table 8.

In the existing works, the best reported values are

- Average insertion loss: 3.8dB @ 15GHz-26GHz
- RMS Gain error: <0.8dB @11GHz-15GHz, RMS phase error:<9.2^o @55GHz-65GHz
- RMS gain error and phase error are not minimized together

The performance of the proposed active quadrature generator based active phase shifter is

- Average Insertion loss: 4.9 dB @ 50GHz-56GHz
- RMS Gain error: <0.86dB @50GHz-56GHz, RMS phase error:<8.64^o @50GHz-56GHz
- Minimize both RMS gain and phase error at the same time

From above, we can infer that the proposed active quadrature generator based active phase shifter achieves the best performance compared to previously reported works at similar frequencies.

Table 8: Performance comparison

Reference	[13]	[33]	[15]	[19]	**Passive phase shifter**	**Passive quad. based. phase shifter**	**Active Quad. based phase shifter**
Frequency (GHz)	11-15	55-65	15-26	30-38	**50-56**	**54-60**	**50-56**
Average gain (dB)	-16.2	-9.4	-3.8	-12	**-16.75**	**-11**	**-4.9**
RMS gain error (dB)	<0.8	-	<2.1	<2.4	**<2.1**	**<1.25**	**<0.86**
RMS phase error (^{o})	<12	<9.2	<13	<7.5	-	**<12**	**<8.64**
Phase range (^{o})	360	180	360	360	**141**	**360**	**360**
Area (mm^2)	4.34	0.2	0.14	0.15	**0.14**	**0.17**	**0.18**
Power (mW)	0	0	11.7	0	**0**	**6**	**23**
Technology	0.18um CMOS	65nm CMOS	0.13um CMOS	0.12um CMOS	**90nm CMOS**	**90nm CMOS**	**90nm CMOS**

CHAPTER VII

LO GENERATION CIRCUITRY

Apart from phase shifters, the LO generation and distribution network form an important part in a phased array system. Since most of the modern transceiver systems are based on super heterodyne architecture, we require a separate IF and LO signal generation circuitry. Also, in systems that support higher modulation schemes like QPSK and n-QAM, a quadrature IF signal is required. This section describes in detail the design of a push-push VCO and QVCO to be used for LO (48GHz) and quadrature IF(13GHz) generation in a phased array system.

7.1 Push Push VCO

7.1.1 Description

In the phased array system, the LO and IF VCO's are frequency locked to a reference frequency by a PLL. Since the LO frequency is 48GHz, the first two divider stages in the PLL need to operate at 48GHz and 24GHz respectively. Though injection locked dividers can be used for frequency division at mmWave frequency, it increases the chip area, complexity and power consumption. To overcome this issue, a push-push VCO(PPVCO) is used to generate both the $2f_o$(48GHz) and f_o at the same time. Here, the $2f_o$ signal can be frequency locked to the desired frequency by locking the f_o signal to the reference signal by a PLL. In a cross-coupled VCO, the common VDD node which combines anti-phase f_o signals is an ideal output port for $2f_o$ signal. Since the VCO core is running at f_o instead of $2f_o$, the gain of the active devices, the quality factor of the transmission lines, the quality factor of the varactor are higher and the current consumption is lower [12]. Since the $2f_o$ output node is a virtual ground for the VCO core, the VCO performance is not affected much by variation of load impedance (load pulling).

7.1.2 Design Procedure

For a cross-coupled VCO to oscillate, the negative resistance of the core needs to be larger than the loss in the tank circuit. Since increasing the size of the cross-coupled pair increases the negative resistance, a large device size is preferred. But, the parasitic capacitance at the output node (large parasitic capacitance degrades tuning range) and the current consumption of the core increase with increase in device size. Hence, an optimum device size that provides enough negative resistance without degrading the tuning range and having a moderate power consumption is considered. After amplification, the $2f_o$ signal is taken out from the common VDD node of the buffer amplifiers. Since the power of the $2f_o$ signal increases with buffer non-linearity, a common source buffer is used instead of a source follower buffer. Also, the VDD of the buffer devices is reduced from 1V to 0.5V to increase the buffer non-linearity [8]. The drain bias for the common source buffers is applied at the common VDD node by using a $\lambda/4$ line at $2f_o$. The $\lambda/4$ line acts as an open at $2f_o$ and 50 ohms at f_o, passing the $2f_o$ signal and attenuating the f_o signal. The schematic of the push-push VCO designed is shown below in Figure 55.

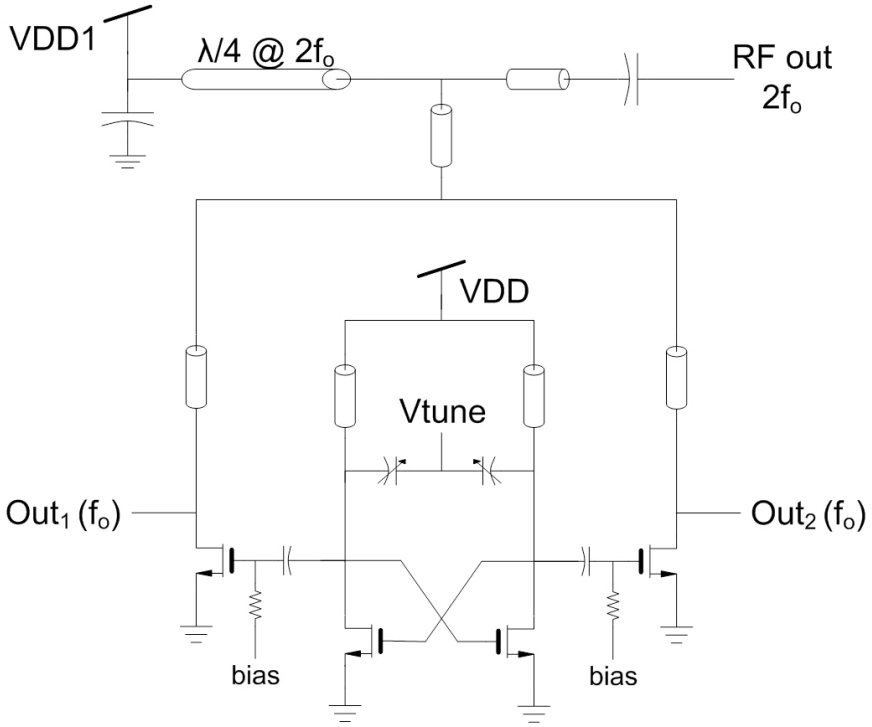


Figure 55: Schematic of push-push VCO

7.1.3 Simulation Results

The layout of the push-push VCO designed is shown below in Figure 56.

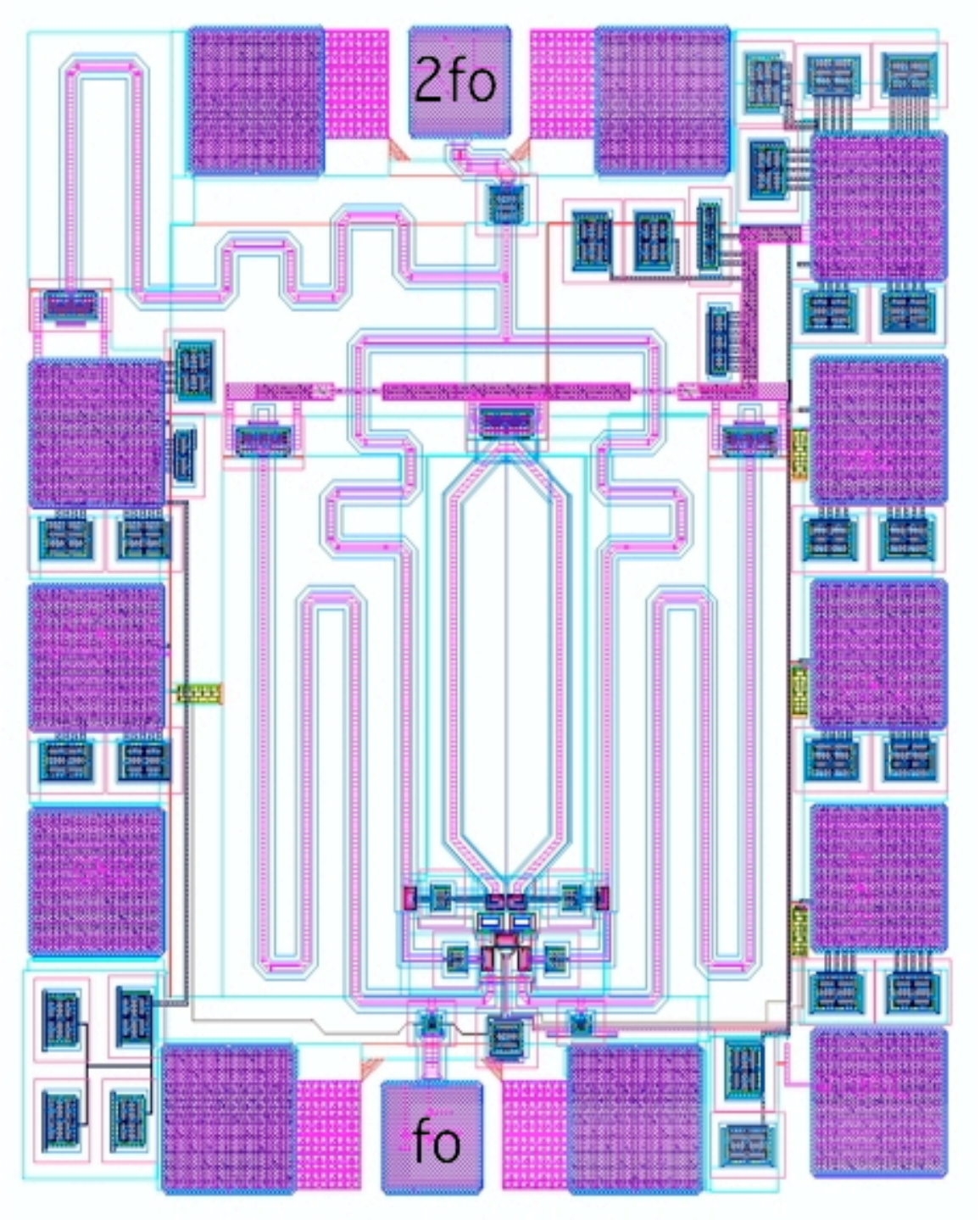


Figure 56: Layout of push-push VCO

The tuning range and the output power level at different vtune values of the PPVCO are shown below in Figure 57 and Figure 58.

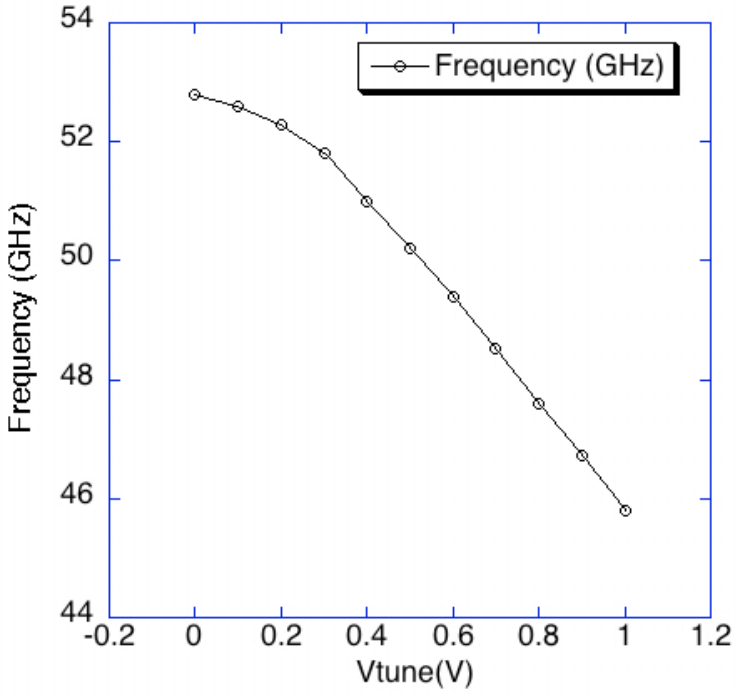


Figure 57: Tuning range of the PPVCO

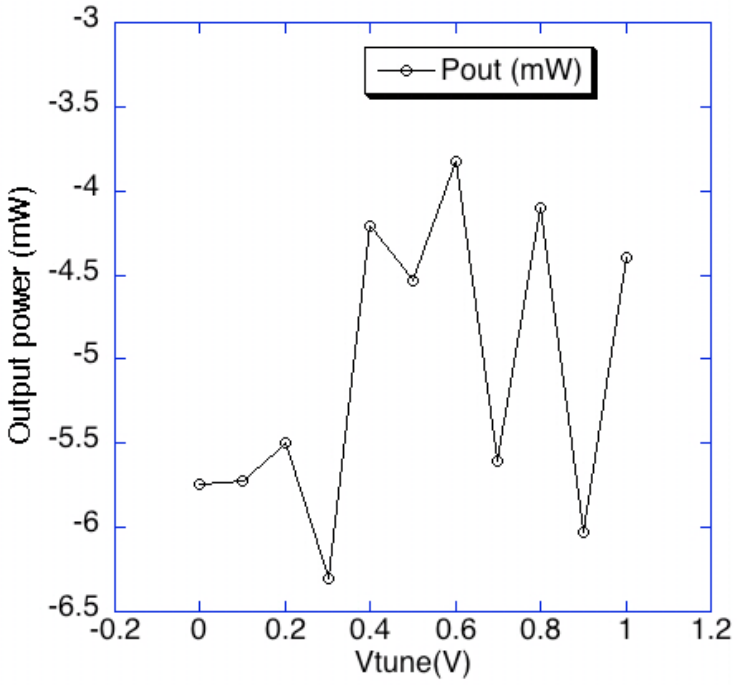


Figure 58: Output power level at different vtune values for a PPVCO

7.1.4 Performance Summary

The complete performance summary of the push-push VCO is shown below in Table 9.

Table 9: Performance summary of PPVCO

Performance parameter	**Result**
Tuning range (GHz)	7(45.8-52.8)
$Pout_{average}$ **@2**f_o **(dBm)**	-5
Phase noise @ 1MHz offset (dBc/Hz)	-83
Area (um^2)	680x780
VDD (V)	1 & 0.5
Power[VCO+buffer] (mW)	45mW
Technology	90nm CMOS

7.2 QVCO

7.2.1 Description

Quadrature LO signals have a wide range of applications. They are used in communication systems for modulation/demodulation of IQ baseband signals, implementation of image rejection filters and for phase interpolation of LO signals by cascading it with a vector modulator. A QVCO consists of two coupled LC VCOs where the injection mechanism forces the output signals to be at quadrature. The coupling between the two cores can be either series or parallel coupling. The designed QVCO use parallel coupling for quadrature generation. The operation of a QVCO can be explained by using a simplified behavioral model [17] shown in Figure 59.

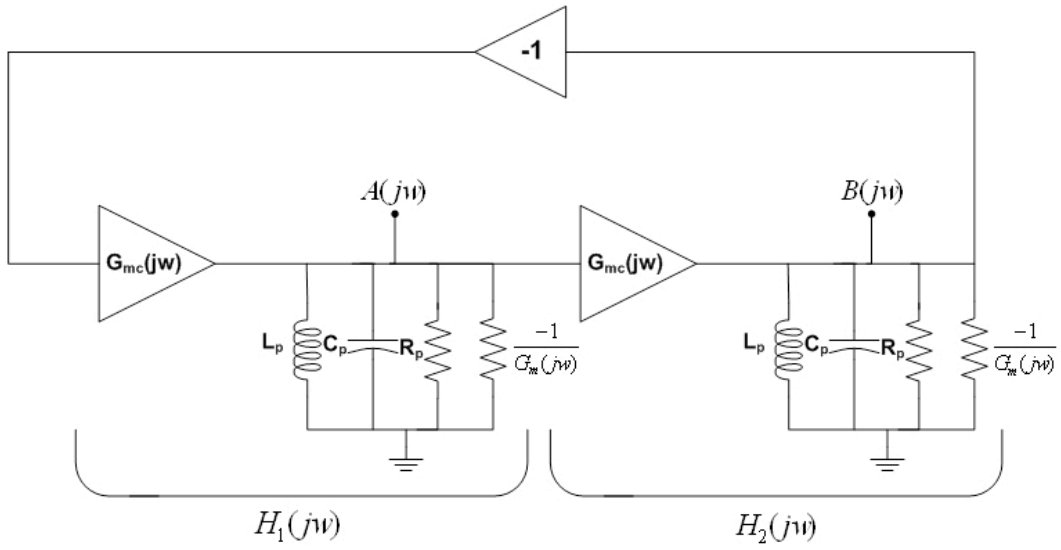


Figure 59: Behavioral model for quadrature VCO

Here, the G_m and G_{mc} represent the large signal transconductance of the cross-coupled core and the coupling devices respectively. Here, L_p, C_p and R_p represent the inductance, the capacitance and the loss in the LC tank circuit respectively. The transfer function for the tank circuit is given below in equation (14).

$$H_{1,2}(jw) = \frac{G_{mc}(jw).jwL_p}{1 + jwL_p\left[\frac{1}{R_p} - G_m(jw)\right] - w^2L_pC_p} \tag{14}$$

$$\alpha = \frac{G_{mc}(jw)}{G_m(jw)} \tag{15}$$

At steady state, the outputs of the two tank circuits are given below.

$$A(jw) = -H_1(jw).B(jw) \tag{16}$$

$$B(jw) = H_2(jw).A(jw) \tag{17}$$

Since $H_1(jw) = H_2(jw)\ and\ A(jw) \neq 0,\ B(jw) \neq 0$

$$A(jw) = \pm jB(jw) \tag{18}$$

Thus, we can infer that the output of the two VCO cores will be at quadrature. Due to coupling between the two cores, the frequency of oscillation, W_{fc}, of the QVCO is slightly away from the free running frequency, W_{fo}, of the tank circuit and is given by the following equation (19) [7].

$$W_{fc} = W_{fo} \pm \frac{G_{mc}}{2C_p} \tag{19}$$

7.2.2 Design Procedure

The designed QVCO consists of two parallel-coupled LC VCOs. The coupling between the cores, and hence the quadrature accuracy, can be improved by increasing the size of the coupling devices. However, the frequency of oscillation, W_{fc}, of the QVCO moves away from the free running frequency, W_{fo}, of the QVCO as given in equation (19). This degrades the phase noise of the QVCO due to reduced quality factor at W_{fc} compared to W_{fo}. Therefore, an optimum-coupling ratio, which provides acceptable quadrature accuracy and phase noise performance, is selected. The optimum size of the cross-coupled devices and the coupling devices chosen is given below in Table 10

Table 10: QVCO device sizing

Device	Width(W), (L=90nm)
Cross-coupled devices	14μm
Coupling devices	3μm

Though the power dissipation can be reduced by ac coupling the coupling devices to the QVCO output, the additional dc blocking capacitors reduce the tuning range by adding parasitic capacitance at the output node. Also, the additional dc blocking capacitors increase the layout complexity. Hence, the designed QVCO uses dc coupling for the coupling

devices. The schematic of the parallel nmos injection QVCO submitted is shown below in Figure 60.

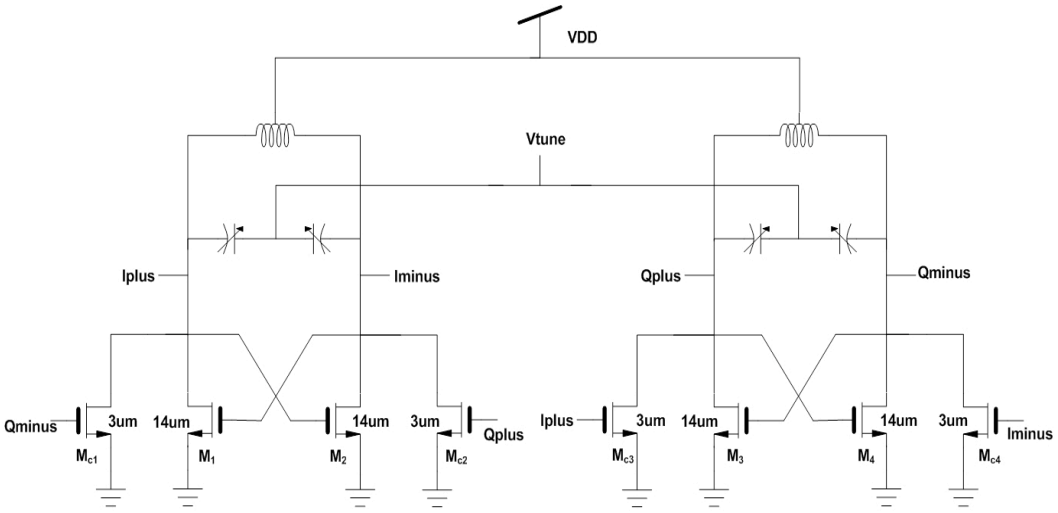


Figure 60: Schematic of quadrature VCO

7.2.3 Simulation Results

The layout of the QVCO designed is shown below in Figure 61.

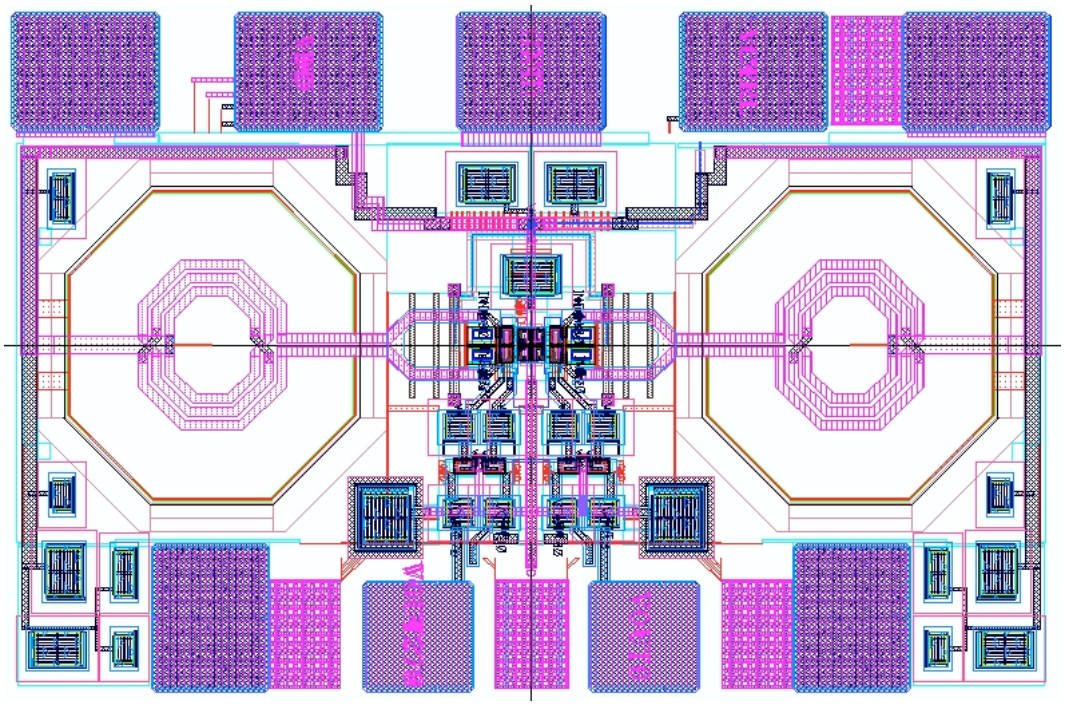


Figure 61: Layout of QVCO

The tuning range of the QVCO is shown below in Figure 62.

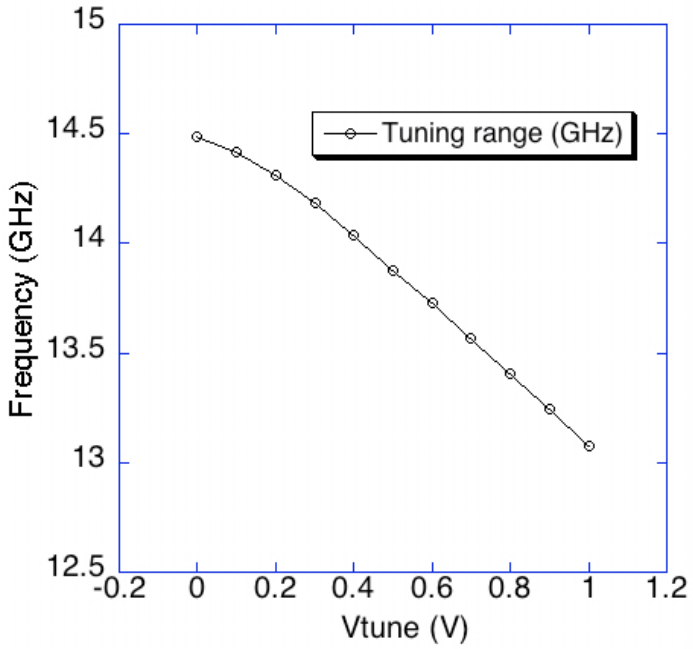


Figure 62: Tuning range of the QVCO

The phase noise of the designed QVCO @ Vtune=0.5V is shown below in Figure 63.

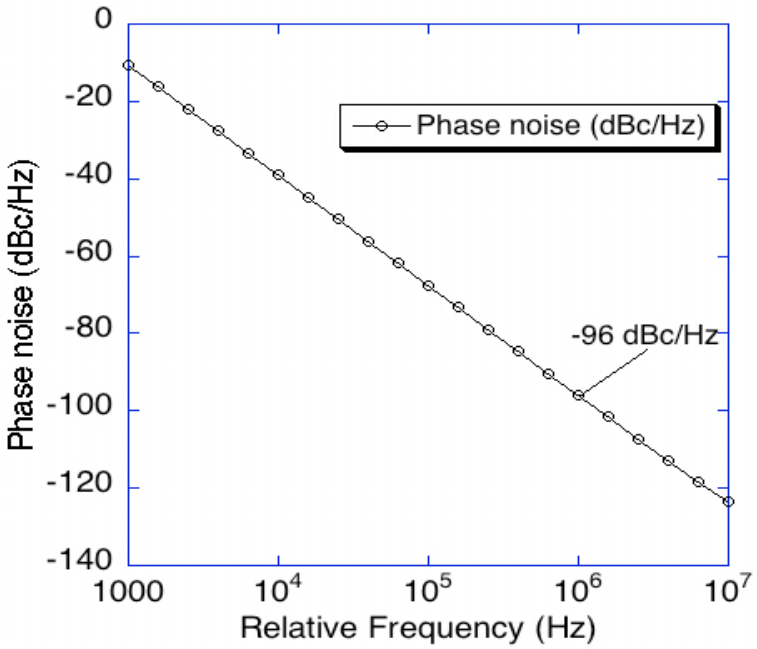


Figure 63: Phase noise of the QVCO @ Vtune=0.5V

7.2.4 Performance Summary

The complete performance summary of the QVCO is shown below in Table 11.

Table 11: Performance summary of QVCO

Performance parameter	**Result**
Tuning range (GHz)	1.4(13.1-14.5)
Single-ended $Pout_{average}$ (dBm)	2.5
Phase noise @ 1MHz offset (dBc/Hz)	-96
Area (um^2)	700x460
VDD (V)	1
Power[VCO+buffer] (mW)	37
Technology	90nm CMOS

CHAPTER VIII

LOW NOISE AMPLIFIER

8.1 Description

Low noise amplifier is an essential component placed in the front end of any wireless receiver system. The total system noise figure and hence the receiver sensitivity is predominantly dependant on the gain and the noise figure performance of the LNA. The linearity of the LNA affects the maximum acceptable input signal level and blocker level, affecting the dynamic range of the system. Since the LNA interacts with the external world, it necessitates a proper matching to 50 ohms at the LNA input. In a direct conversion receiver, a good input matching ensures proper operation of the receiver antenna. In a super heterodyne receiver, the insertion loss and band rejection performance of the image rejection filter is dependant on the impedance presented by the LNA. Since a mixer, which is driven by a very high power LO, usually follows the LNA, the reverse isolation of the LNA determines the maximum in-band (direct conversion receiver) and out-of-band (super heterodyne receiver) emission from the receiver antenna. The above parameters are tabulated below in Table 12.

Table 12: Performance parameters for LNA

Performance parameter	**System parameters affected**	**Target Specs**
Noise Figure (dB)	Total NF, Sensitivity	< 8
Gain (dB)	Total NF, Mixer P1dB	>20
Input matching (dB)	Performance of image reject filter and antenna	<-10
Input P1dB (dBm)	Maximum input and blocker level	>-25
Reverse isolation (dB)	Emission from RX antenna	>40
Power (mW)	Total power budget	<70

8.2 Design Procedure

The designed LNA consists of a four-stage common source amplifier with inductive degeneration in the 1st stage. The four-stage design is chosen to obtain a gain more than 20dB over a large bandwidth. Since the noise figure performance of an amplifier is optimum for a particular current density, which varies with technology, the current density in each device is selected to be 0.3mA/um [4], [6]. To improve the linearity of the circuit without considerable power consumption, the first two stages are chosen to be of 40um wide and the last two stages to be 60um wide. Inductive source degeneration is added to the first stage to improve the noise figure performance and to bring the noise optimum impedance and the power optimum impedance close together. Also, the addition of inductive degeneration widens the range of frequencies for which the minimum noise figure performance is obtained. The schematic of the designed low noise amplifier is shown below in Figure 64.

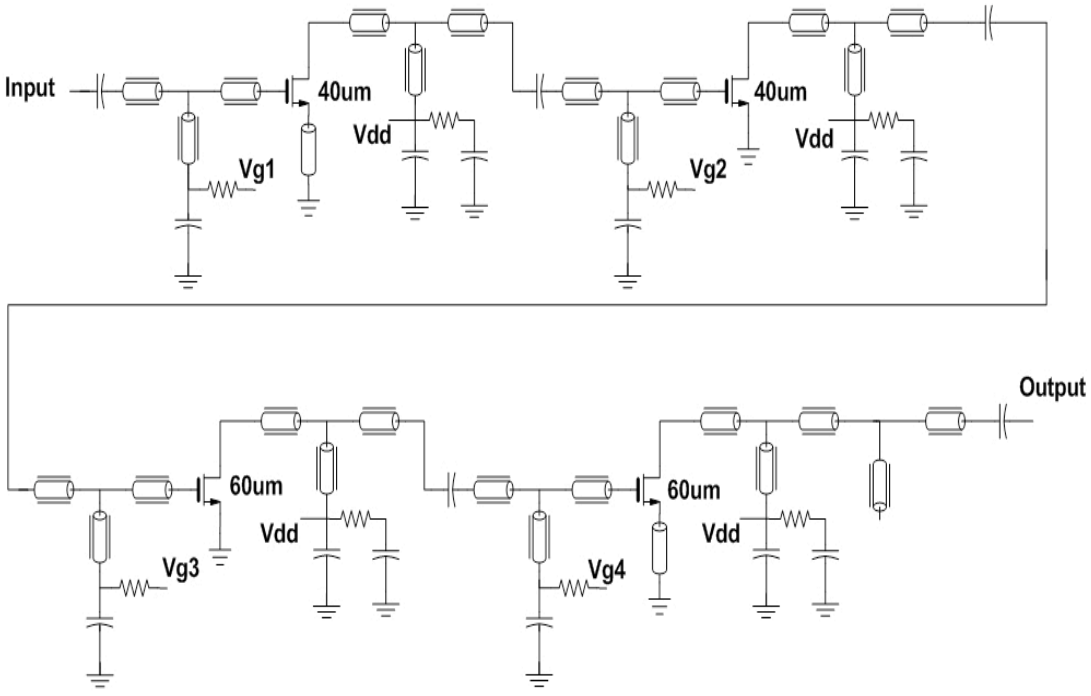


Figure 64: Schematic of low noise amplifier

8.3 Simulation Results

The layout of the low noise amplifier is shown below in Figure 65.

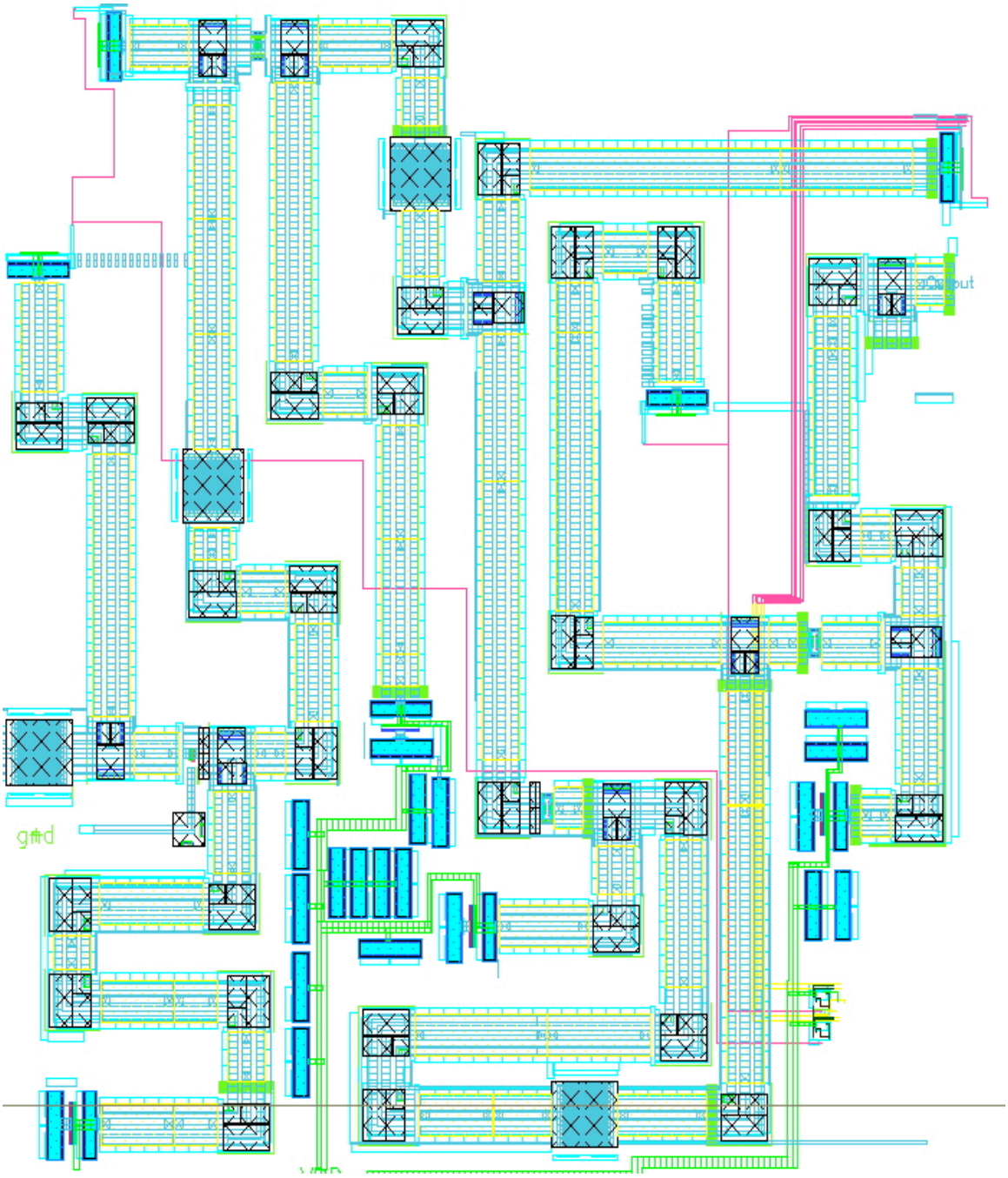


Figure 65: Layout of low noise amplifier

The input and output matching for the designed low noise amplifier are shown below in Figure 66.

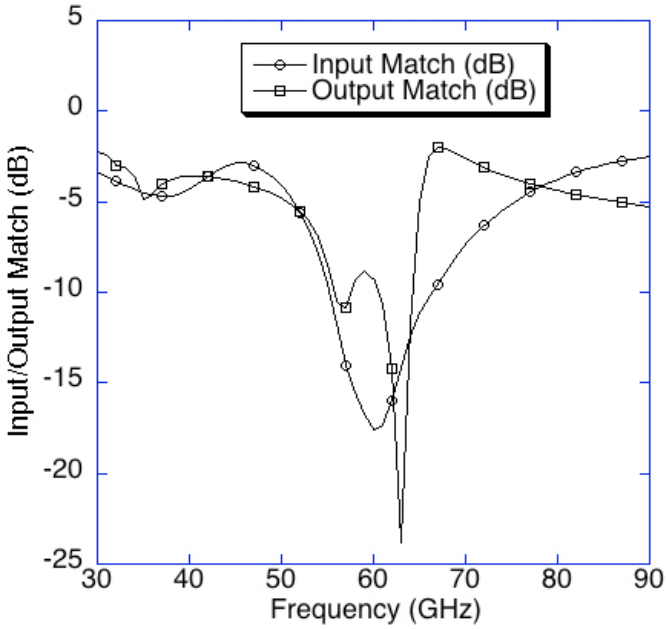


Figure 66: Input and output matching of low noise amplifier

The gain and isolation of the designed low noise amplifier are shown below in Figure 67.

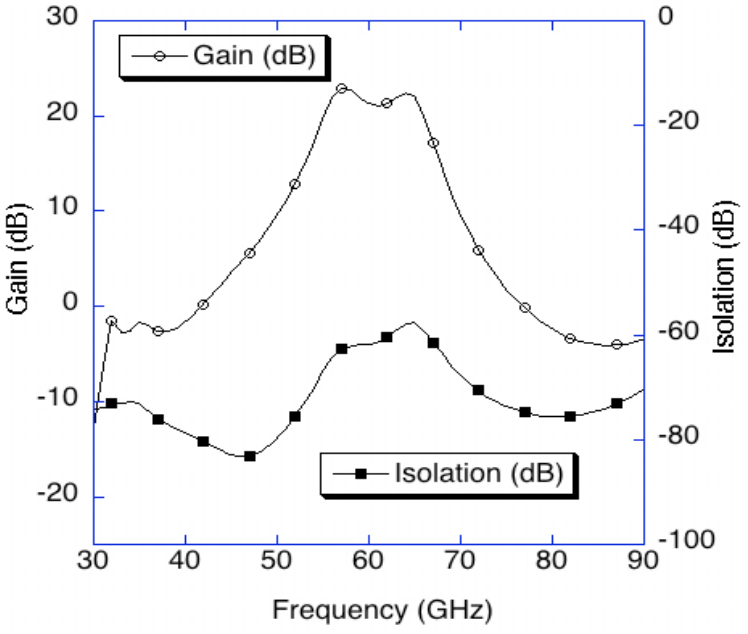


Figure 67: Gain and isolation of low noise amplifier

The stability of the LNA is ensured by verifying that the small signal stability factor, kf is above 10 over the entire frequency range from 0 to 100GHz. The noise figure and stability factor of the low noise amplifier are shown below in Figure 68.

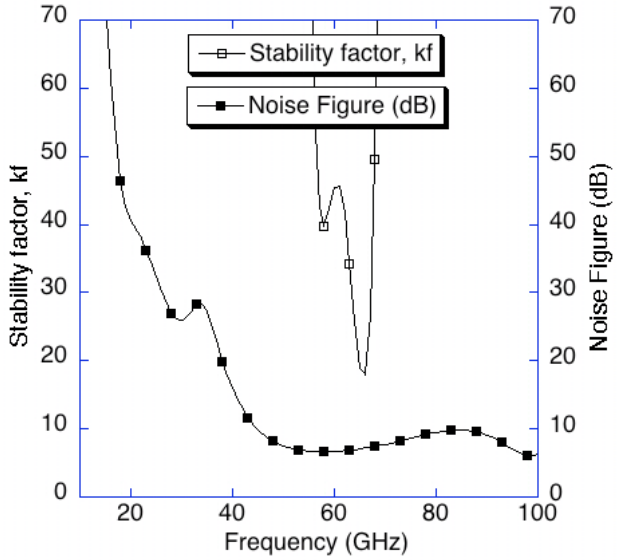


Figure 68: Noise figure and stability factor of low noise amplifier

8.4 Performance Summary

The complete performance summary of the low noise amplifier is shown below in Table 13.

Table 13: Performance summary of LNA

Performance parameter	**Result**
Input Match (less than -10dB, GHz)	55-67
Gain (dB)	23
NF (dB)	6.7
IP1dB (dBm)	-21
Stability factor, kf	>18
Area (um^2)	880x800
Power (mW)	60
Technology	45nm CMOS SOI

8.5 Tunable Transmission line for LNA

8.5.1 Description

With the emergence of multiple frequency standards in mmWave, there is a need for wide-band mmWave systems. Since the fractional bandwidth of mmWave systems is usually less than 0.2, tunable elements can be used to extend the useable bandwidth, enabling operation at multiple frequency bands. A tunable transmission line is one such component whose characteristic impedance and phase can be varied by an external control signal. These characteristics are usually obtained by varying the distance between the signal line and ground line [9]. Here, connecting the bottom metal line to the ground by turning on a switch or leaving it floating by turning off a switch varies the distance between the signal and the ground lines. The schematic of a tunable transmission line implemented is shown below in Figure 69.

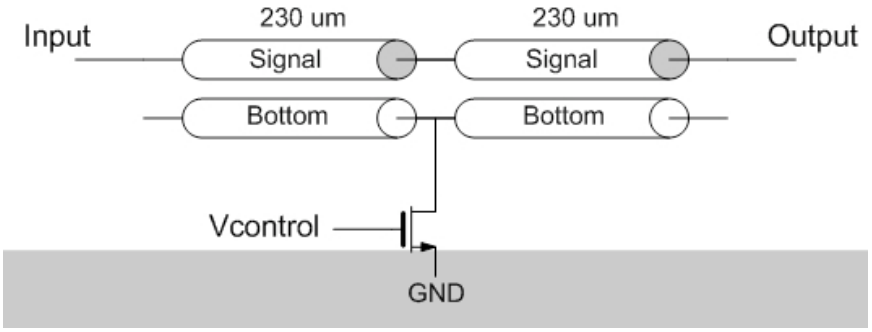
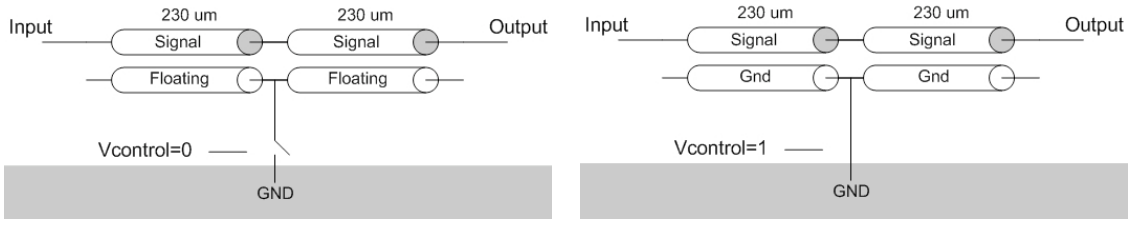


Figure 69: Schematic of the tunable transmission line

The simplified schematic of the tunable transmission line for Vcontrol =0V and Vcontrol=1V is shown below in Figure 70(a) and Figure 70(b)



(a) Vcontrol=0 (b) Vcontrol=1

Figure 70: Simplified schematic for (a) Vcontrol=0 and (b) Vcontrol=1

8.5.2 Simulation Results

The layout of the tunable transmission line is shown below in Figure 71.

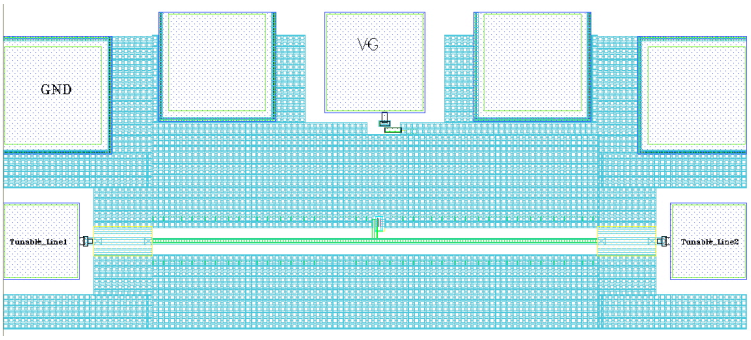
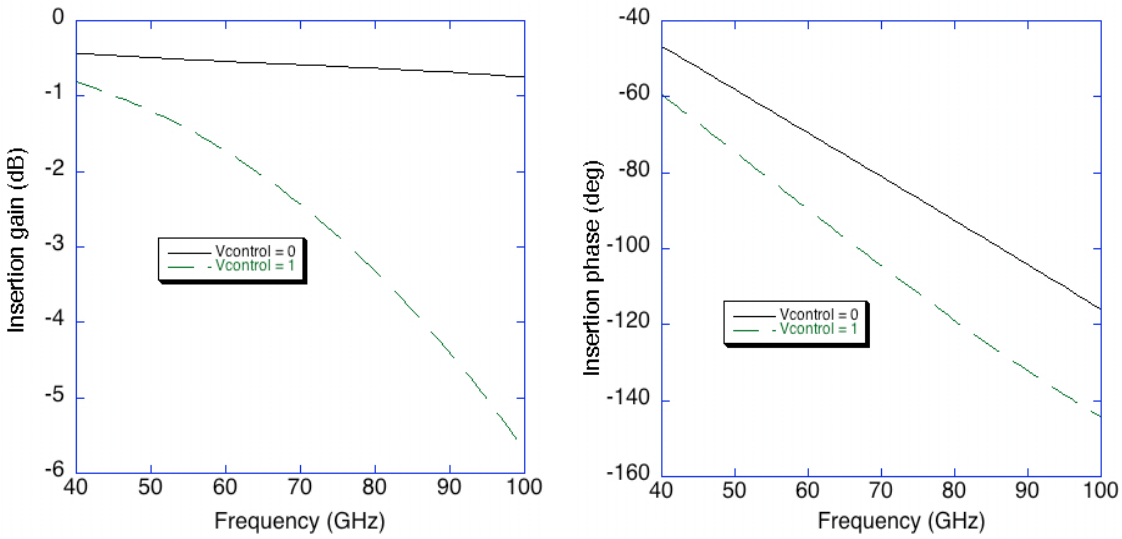


Figure 71: Layout of the tunable transmission line

The variation of insertion loss and insertion phase of the tunable tline for Vcontrol =0V and Vcontrol=1V is shown below in Figure 72(a) and Figure 72(b).



(a) Insertion loss

(b) Insertion phase

Figure 72: (a) Insertion loss and (b) Insertion phase variation of the tunable transmission line

Table 14: Performance summary of tunable transmission line

Frequency (GHz)	80
Phase variation (^{o})	26

CHAPTER IX

CONCLUSION

9.1 List of Important Features and Innovations

- Proposed a novel active quadrature generation scheme which can be used for quadrature generation and phase shifting [30].
- The novel active quadrature generator based active phase shifter has the best performance compared to other reported works at similar frequencies [Refer Table 8].
  - ⋆ Maximum gain
  - ⋆ Minimum RMS gain error and RMS phase error
  - ⋆ 360^o continuous phase tuning range (@ V-band)
  - ⋆ Balanced quadrature output signals
- A comprehensive study and design of passive and active phase shifters at mmWave frequencies are presented [30].
- Proposed a novel IF phase shifter based phased array system that can be used for scalable phased array system [22].
- Proposed a novel PLL based phase shifting approach which can be used for IF and LO phase shifter based phased array systems [29].
- The design of different LO generation circuitries at mmWave frequencies is discussed.
- The design of low noise amplifier at 60GHz and methods to increase their useable bandwidth is discussed.
- The techniques used for modeling at mmWave frequencies are discussed.

9.2 Summary

The different phased array system architectures available in literature are discussed. A novel PLL phase shifter and IF phase shifter based phased array systems are proposed here. The design of mmWave components like phase shifter, LNA and LO generation circuitry for a phased array system are discussed in this thesis.

9.3 Scope for Future Work

Other mmWave front-end components such as mixer, IF amplifier can be implemented and integrated with the designed circuits to form a complete CMOS mmWave phased array system. The LO phase shifters can also be used for IF and RF phase shifter based phased array systems. The designed PPVCO and QVCO can be integrated with a PLL and used for synthesis of required output frequency. Using tunable elements, the designed LNA can be used for multi frequency bands. A complete beam former algorithm can be developed to enable automation of phased array measurement.

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